METHODIST
COLLEGE OF ENGINEERING AND TECHNOLOGY
Approved by AICTE New Delhi | Affiliated to Osmania University, Hyderabad
Abids, Hyderabad, Telangana, 500001

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IC APPLICATIONS LABORATORY

STUDENT LABORATORY MANUAL

(As per 2021-2022 Academic Regulations)

B.E V SEMISTER E&CE

SUBJECT CODE: PC 551 EC

Name:_____

Roll No.:_____

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Prepared by

Mr. P. Ramesh Babu, Assistant Professor
Mr. D. Suresh, Assistant Professor

Methodist College of Engineering & Technology

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Experiment No.	Title of the Experiment	Date	Page No.	Marks				Remarks/ Signature
				E	O	R	T	
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E: Experiment (10 Marks) **O: Observation (10 Marks)** **R: Record (5Marks)** **T: Total (25 Marks)**

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision of the Institute:

To produce ethical, socially conscious and innovative professionals who would contribute to sustainable technological development of the society.

Mission of the Institute:

To impart quality engineering education with latest technological developments and interdisciplinary skills to make students succeed in professional practice

To encourage research culture among faculty and students by establishing state of art laboratories and exposing them to modern industrial and organizational practices

To inculcate humane qualities like environmental consciousness, leadership, social values, professional ethics and engage in independent and lifelong learning for sustainable contribution to the society

Vision of the Department:

To strive to become centre of excellence in Education, Research with moral, ethical values and serve society

Mission of the Department:

M1: To provide Electronics & Communication Engineering knowledge for successful career either in industry or research

M2: To develop Industry-Interaction for innovation, product oriented research and development.

M3: To facilitate value added education combined with hands-on trainings

Program Educational Objectives:

PEO 1: Apply the knowledge of Basic sciences and Engineering in designing and implementing the solutions in emerging areas of Electronics and Communication Engineering.

PEO 2: Pursue the research or higher education and practise profession.

PEO 3: Adapt to the technological advancements for providing the sustainable Engineering solutions to meet organisation/society needs

PEO 4: Work as an individual or in a team with professional ethics and values.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Program Outcomes:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):

PSO1: Professional Competence: Apply the knowledge of Electronics & Communication Engineering principles in different domains like VLSI, Signal processing, Communication, Embedded system & Control Engineering.

PSO2: **Technical Skills**: Able to design and implement products using the cutting- edge software and hardware tools and hence provide simple solutions to complex problems.

PSO3: Social consciousness: Graduates will be able to demonstrate the leadership qualities and strive for the betterment of organization, environment and society

Estd : 2008

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LAB INSTRUCTIONS

Lab Rule of conduct, DO's & DON'Ts

Conduct yourself in a responsible manner at all times in the laboratory. Don't talk aloud or crack jokes in lab.

A lab coat should be worn during laboratory experiments.

Dress properly during a laboratory activity. Long hair, dangling jewellery and loose or baggy clothing are a hazard in the laboratory.

Observe good housekeeping practices. Replace the materials in proper place after work to keep the lab area tidy.

Do not wander around the room, distract other students, startle other students or interfere with the laboratory experiments of others.

Do not eat food, drink beverages or chew gum in the laboratory and do not use laboratory glassware as containers for food or beverages.

Rules & Guidelines for conducting Lab-Work

Students are not allowed to touch any equipment, in the laboratory area until you are instructed by Teacher or Technician.

Before starting Laboratory work follow all written and verbal instructions carefully. If you do not understand a direction or part of a procedure, ASK YOUR CONCERNED TEACHER BEFORE PROCEEDING WITH THE ACTIVITY.

Before use equipment must be read carefully Labels and instructions. Set up and use the equipment as directed by your teacher. If you do not understand how to use a piece of equipment, ASK THE TEACHER FOR HELP!

Perform only those experiments authorized by your teacher. Carefully follow all instructions, both written and oral. Unauthorized experiments are not allowed in the Laboratory. Students are not allowed to work in Laboratory alone or without presence of the teacher. Any failure / break-down of equipment must be reported to the teacher. Protect yourself from getting electric shock.

Estd : 2008

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	Course Code	**Course Title**						**Core/ Elective**
	PC551EC	**IC APPLICATIONS LAB**						Core
	Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	LICA PC 501EC STLD PC302EC	L	T	D	P			
		-	-	-	2	25	50	1

Course Objectives:
Design and analyze the various linear application of Op-amp.
Design and analyze the active filters circuit using Op-amp.
Design and analyze oscillators and Multivibrators using Op-amp & 555.
Design sequential circuits- Counters &Registers.

Course Outcomes:
Implement operational amplifiers Linear & Non-linear circuits.
Implement Active filters using Op-amps.
Implement oscillators, Multivibrators, etc., using Op-amps.
Illustrate sequential circuits – Counters & Registers

PART- A

1. Measurement of op-Amp. Parameters, Voltage follower.
2. Inverting and non- Inverting amplifiers using Op-Amp.
3. Integrator Differentiator circuits using Op-Amp.
4. Active filters: LP, HP and BP filters using Op-Amp.
5. Clipper and clamper circuit using Op-Amp.
6. Triangular wave generator using Op-Amp.
7. Monostable and Astable multivibrator using Op-Amp.
8. Monostable and Astable multivibrator using 555 Timer.
9. IC voltage regulator.
10. Voltage controlled oscillator – NE 565
11. Four bit ADC and DAC using Op Amp

PART - B

1. Flip Flop conversions and latches using gates and ICs.
2. Designing Synchronous, Asynchronous up/ down counters.
3. Shift Registers and Ring counters using IC Flip-Flop & Standards IC counters.
4. Interfacing counters with 7-segment LED /LCD display units.
5. Mux – Demux applications.

Note: Atleast ten experiments should be conducted in the semester, of which three should be from PART - B.

Suggested Readings:

1. D.RoyChowdhary, B.JainShail - Linear Integrated circuit, 4th Edition.
2. Jain R.P., "Modern Digital Electronics" 3/e TMH 2003.

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INTRODUCTION

IC 741 Op Amp Basics, Characteristics, Pin Configuration, Applications

Introduction to Operational Amplifiers

An operational amplifier, also called as an op-amp or op amp, is an integrated circuit primarily designed for performing analogue computations. It has a very high voltage gain, typically of the order of 104 (100dB).

Although they are specially designed for performing operations like addition, subtraction, integration, differentiation etc., by using external components like resistors and capacitors to create a required feedback mechanism, it can also be used as an amplifier and for many other functions like filters, comparators etc.

Op-Amp IC's have become an integral part of almost all analogue circuitry. In this article we will take a look at one of the most used Op-Amp ICs: IC 741 Op Amp.

IC 741 Op Amp (Operational Amplifier)

The 741 Op Amp IC is a monolithic integrated circuit, comprising of a general purpose Operational Amplifier. It was first manufactured by Fairchild semiconductors in the year 1963. The number 741 indicates that this operational amplifier IC has 7 functional pins, 4 pins capable of taking input and 1 output pin.

IC 741 Op Amp can provide high voltage gain and can be operated over a wide range of voltages, which makes it the best choice for use in integrators, summing amplifiers and general feedback applications. It also features short circuit protection and internal frequency compensation circuits built in it. This Op-amp IC comes in the following form factors:

Pinout of IC 741 Op Amp and their Functions

Fig. A illustrates the pin configurations and internal block diagram of IC 741 in 8 pin DIP package.

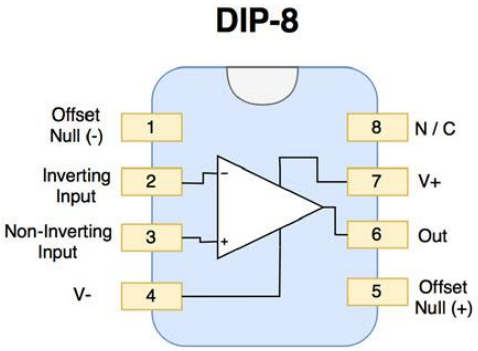


Fig. A: Pin Configuration of IC 741 Op Amp

Pin4 & Pin7 (Power Supply): Pin7 is the positive voltage supply terminal and Pin4 is the negative voltage supply terminal. The 741 IC draws in power for its operation from these pins. The voltage between these two pins can be anywhere between 5V and 18V.

Pin6 (Output): This is the output pin of IC 741. The voltage at this pin depends on the signals at the input pins and the feedback mechanism used. If the output is said to be high, it means that voltage at the output is equal to positive supply voltage. Similarly, if the output is said to be low, it means that voltage at the output is equal to negative supply voltage.

Pin2 & Pin3 (Input): These are input pins for the IC. Pin2 is the inverting input and Pin3 is the non-inverting input. If the voltage at Pin2 is greater than the voltage at Pin3, i.e., the voltage at inverting input is higher, the output signal stays low. Similarly, if the voltage at Pin3 is greater than the voltage at Pin2, i.e., the voltage at non-inverting input is high, the output goes high.

Pin1 & Pin5 (Offset Null): Because of high gain provided by 741 Op-Amp, even slight differences in voltages at the inverting and non-inverting inputs, caused due to irregularities in manufacturing process or external disturbances, can influence the output. To nullify this effect, an offset voltage can be applied at pin1 and pin5, and is usually done using a potentiometer.

Pin8 (N/C): This pin is not connected to any circuit inside 741 IC. It's just a dummy lead used to fill the void space in standard 8 pin packages.

Specifications

The following are the basic specifications of IC 741:

Power Supply: Requires a Minimum voltage of 5V and can withstand up to 18V

Input Impedance: About 2 MΩ

Output impedance: About 75 Ω

Voltage Gain: 200,000 for low frequencies

Maximum Output Current: 20mA

Recommended Output Load: Greater than 2 kΩ

Input Offset: Ranges between 2mV and 6mV

Slew Rate: 0.5V/microsecond (It is the rate at which an Op-Amp can detect voltage changes)

The high input impedance and very small output impedance makes IC 741 a near ideal voltage amplifier.

Applications

Following are the applications of IC 741 Op Amp across different use cases:

Amplifiers: 741 IC is mostly used to amplify signals of varying frequencies ranging from DC to higher radio frequencies. It is also used in frequency selective amplifiers which filter out signals of unwanted frequencies, E.g. tone control systems in stereo and Hi Fi systems.

Computational: Many electronic circuits that perform mathematical operations like integration, differentiation, summers etc. use 741 Op-Amp.

Rectifiers: Ordinary diodes used in rectifiers have voltage drop across them which makes it unsuitable for high accuracy signal rectifiers. The 741 IC can be configured to perform as an ideal diode i.e., with no voltage drop at all and can be used in precise rectifier circuits.

Oscillators: Op-Amp IC 741 is used as an oscillator in function generators to create different output waveforms like sinusoidal, square, triangular etc. It is also used in Pulse Width Modulators (PWM generators)

Comparators: The 741 IC can be used to compare voltage signals and determine if they are almost of the same voltage. This can be used in voltage regulators and signal comparators.

ADCs / DACs: 741 Op-Amp can be used to create Digital to Analogue Converters that can take digital binary input from computers or microcontrollers and create a corresponding analogue signal. Similarly, it is can also used in Analogue to Digital circuits.

The typical parameters of a 741 IC

Parameters	Typical Range	Ideal Value
Open Loop Gain(A)	10^5 to 10^8	$\propto$
Input Resistance(R_i)	10^5 to 10^{13}	$\propto$
Output Resistance(R_o)	10 to 100	0

IC 555 Timer Working: Pin Diagram & Specifications

The 555 timer IC is an integral part of electronics projects. Be it a simple project involving a single 8-bit micro-controller and some peripherals or a complex one involving system on chips (SoCs), 555 timer working is involved. These provide time delays, as an oscillator and as a flip-flop element among other applications.

Introduced in 1971 by the American company Signetics, the 555 is still in widespread use due to its low price, ease of use and stability.

Fig. B shows the pin diagram of the timer IC 555 and Table A shows the description of the various pins of timer IC 555.

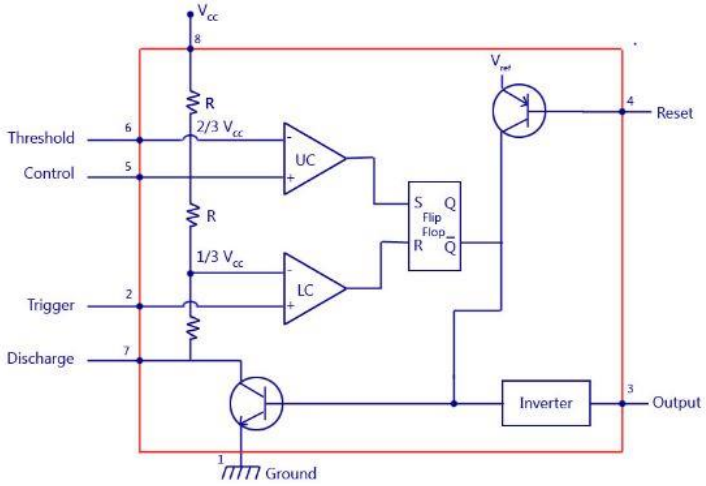


Fig. B: Pin Diagram of IC 555

Table A: Pin diagram and description		
Pin	**Name**	**Purpose**
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 *V*cc, CTRL being 2/3 *V*cc by default if CTRL is left open). In other words, OUT is high as long as the trigger low. Output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.
3	OUT	This output is driven to approximately 1.7 V below +*V*cc, or to GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides threshold.
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 *V*cc).
6	THR	The timing (OUT high) interval ends when the voltage at threshold is greater than that at CTRL (2/3 *V*cc if CTRL is open).
7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with output.
8	*V*cc	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

Some important features of the 555 timer:

555 timer is used in almost every electronic circuit today. For a 555 timer working as a flip flop or as a multi-vibrator, it has a particular set of configurations. Some of the major features of the 555 timer would be,

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.

- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohertz.
- The output of a 555 timer can drive transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature which is equivalent to 0.005 %/ °C.
- The duty cycle of the timer is adjustable.
- Also, the maximum power dissipation per package is 600 mW and its trigger and reset input has logic compatibility.

555 timer working:

The 555 generally operates in 3 modes: A-stable, Mono-stable, Bi-stable modes.

Astable mode

This means there will be no stable level at the output. So the output will be swinging between high and low. This character of unstable output is used as a clock or square wave output for many applications.

Mono-stable mode

This configuration consists of one stable and one unstable state. The stable state can be chosen either high or low by the user. If the stable output is set at high (1), the output of the timer is high (1). At the application of an interrupt, the timer output turns low (0). Since the low state is unstable it goes to high (1) automatically after the interrupt passes. Similar is the case for a low stable monostable mode.

Bi-stable mode

In bistable mode, both the output states are stable. At each interrupt, the output changes from low (0) to high (1) and vice versa, and stays there. For example, if we have a high (1) output, it will go low (0) once it receives an interrupt and stays low (0) till the next interrupt changes the status.

Experiment –1

Measurements of OP-AMP parameters, Voltage follower

Measurements of OP-AMP parameters

Aim:

To measure the parameters of op-amp such as Input bias current, Input offset current, Input and Output offset voltage and Slew rate

Equipments/ Components Required:

Components:

Name	Specifications/ Range	Quantity
Op-amp	µA741C	1
Resistor	100Ω, ¼ W	2
	10k, ¼ W	2
	100k, ¼ W	1
Capacitor	0.01µF	2

Equipments:

Name	Specifications/ Range	Quantity
IC Trainer board		1
Digital ammeter	0-200µA/200mA	1
Digital voltmeter	0-2V/20V	1
Function generator	0-20MHz.	1
Dual trace CRO	0-200MHz	1
DC Power supply		1

Theory:

The µA741 device is a general-purpose operational Short-Circuit Protection amplifier featuring offset-voltage null capability.

Input bias current: The inverting and non-inverting terminals of an op-amp are actually two base terminals of transistors of a differential amplifier. In an ideal op-amp it is supported that no current flows through these terminals. However, practically a small amount of current flows through these terminals which is on the order of nA (typical and maximum values are 80 and 1500nA) in bipolar op-amps and pA for FET op-amps.

Input bias current is defined as the average of the currents entering into the inverting and non-inverting terminals of an op-amp. To compensate for bias currents a compensating resistor R_{comp} is used. Value of R_{comp} is parallel combination of the resistors connected to the inverting terminal.

Input bias current $I_B = (I_{B1}+I_{B2}) / 2$

where I_{B1} and I_{B2} are the base bias currents of the op-amp.

Input offset current: Input offset current is defined as the algebraic difference between the currents into the inverting and non-inverting terminals.

$$Ios = |I_{B1}-I_{B2}|$$

where I_{B1} and I_{B2} are the base bias currents of the op-amp. The bias currents IB1 and IB2 will not be equal in an op-amp.

Typical and maximum values of input offset current are 20nA and 200nA, respectively.

Input offset voltage: Even if the input voltage is zero, output voltage may not be zero. This is because of the circuit imbalances inside the op-amp. In order to compensate this, a small voltage should be applied between the input terminals. Input offset voltage is defined as the voltage that must be applied between the input terminals of an op-amp to nullify the output voltage. Typical and maximum values of input offset voltage are 2mV and 6mV, respectively.

Slew rate: Slew rate is the rate of rise of output voltage. It is the measure of fastness of op-amp. It is expressed in V/μsec. If the slope requirements of the output voltage of the op-amp are greater than the slew rate, distortion occurs. Slew rate is measured by applying a step input voltage.

Output offset voltage: The voltage existing at the output when inputs are zero due to input offset voltage & bias current is called output offset voltage. Ideally it is zero when both input op-amp zero. It is only produced due to input offset voltage and bias current.

Circuit Diagram: Measurement of Input and Output offset voltage

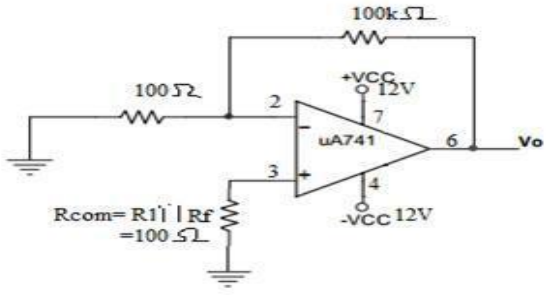


Fig.1.1: Circuit Diagram to measure input and output offset voltage

Procedure:-

1. Connect the circuit as shown in Fig.1.1
2. Measure Output voltage i.e; Output offset voltage (V_{oo}).
3. Calculated Input offset voltage from Vio = Voo / (1+Rf/R1)

Circuit Diagram: Measurement of Input bias current and Input offset current

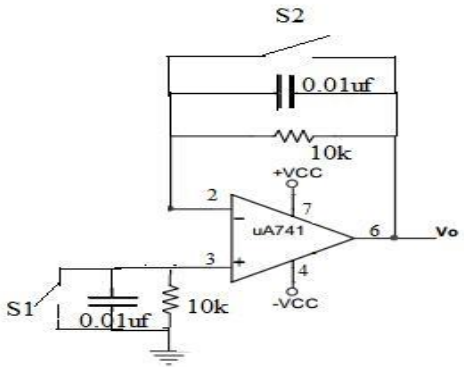


Fig.1.2: Circuit Diagram to measure Input bias current and Input offset current

Procedure:-

1. Connect the circuit as shown in Fig.1.2.
2. Close the switch S1 and measure Output voltage.
3. Using the value of output voltage, calculate I_{B2}
3. Now Close the switch S2 and measure Output voltage.
4. Using the value of output voltage, calculate I_{B1}
5. Using the values of I_{B1} & I_{B2}, Calculate Input bias current and Input offset current using

$$I_B=|I_{B1}+I_{B2}|/2; \qquad Iio =|I_{B1}| -|I_{B2}|$$

Circuit Diagram: Measurement of slew rate

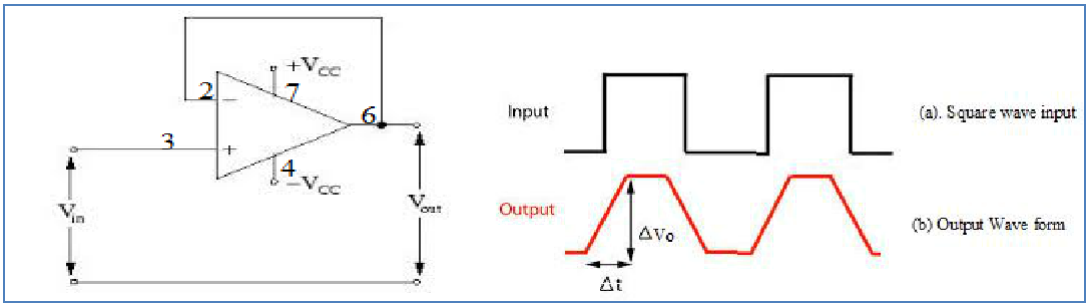


Fig.1.3: Circuit Diagram to measure slew rate

Procedure:-

1. Connect unity gain amplifier circuit as shown in Fig. 1.3

2. Apply Square wave as input having magnitude 1 V (p-p) and frequency 1 KHz
3. Observe Output waveform by varying freq of input from 1 kHz to higher value
4. Slew rate is calculated using Slew Rate = $\Delta Vo/\Delta t$

Observations & Calculations:

1. Voo=…….

   Vio = Voo / (1+Rf/R1)

2. Vo_2=……..

   I_{B2} = Vo/10K

   Vo1=…….

   I_{B1} = Vo_1/10K.

   $I_B=|I_{B1}+I_{B2}|/2$

   Iio =$|I_{B1}|$ -$|I_{B2}|$

3. ΔVo…
   ..V
   Δt=…μ
   sec
   Slew
   rate=…
   …….

Result:

The input bias current, input offset current, input offset voltage and slew rate of the op-amp were determined.

4.
Input offset voltage = ……..mV

Input bias current = ……...A

Input offset current = ...…...A

Slew rate = ……..V/μs.

EXPERIMENT-2

Inverting and non- Inverting amplifiers using Op-Amp

Aim:-

1. To design an inverting amplifier using op-amp with gain of -10.
2. To design a non-inverting amplifier using op-amp with gain of 11.
3. To realize a voltage follower using op-amp.

Equipments / Components Required:

Components:

Name	Specifications/ Range	Quantity
Op-amp	μA741C	1
Resistor	100Ω	2
	10k Ω	1
	100k Ω	1

Equipment:

Name	Specifications/ Range	Quantity
IC Trainer board		1
Function generator	0-20MHz.	1
Dual trace CRO	0-200MHz	1
DC Power supply		

THEORY:

INVERTING AMPLIFIER:

In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **"Virtual Earth"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Design Of Inverting Amplifier:-

The gain of an inverting amplifier is given by $A_v = V_o / V_{in} = - R_f / R_1$

Given that $A_v = - 10$

Assume that R_1=10KΩ

Therefore, $R_f = A_v.R_1 = -10 \times 10 \times 10^3 = 100K\Omega$

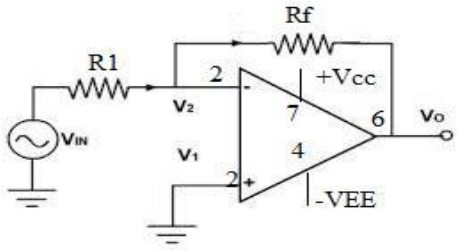


Fig.2.1: Inverting Amplifier

Procedure:-

1. Connect the circuit as per the circuit diagram shown in Fig.2.1
2. Apply sine wave as input with the magnitude of 1V (p-p) and frequency 1 KHz
3. Observe the output wave and note down the amplitude of output voltage.
4. Compare the practical value of V_o with its theoretical value.
5. Calculate the gain of the amplifier using $A_v = - V_o / V_i$.

Observations:

V_i = 1 V (p-p), f_i = 1 KHz

Sl. No.	Output voltage V_o (Volts) Practical	Output voltage V_o (Volts) Theoretical	Gain
1			

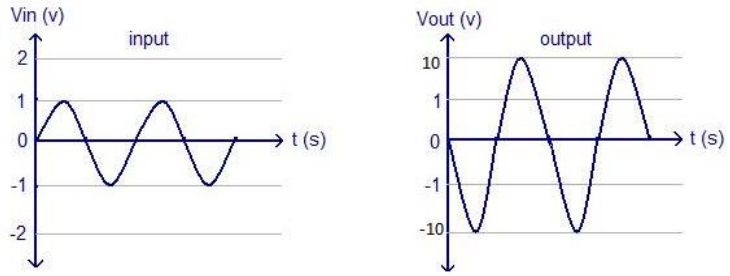


Fig. 2.2: Input and Output wave forms of an Inverting amplifier

Non- Inverting Amplifier:-

In this configuration, the input voltage signal, (V_{IN}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a R*f* – R2 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, very high input impedance, R_{in} approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and low output impedance, Rout.

Design Of Non-Inverting Amplifier:-

Gain of an inverting Amplifier is given by $A_v = V_o / V_{in} = 1 + R_f / R_1$

Given that A_v =11

Assume that R_1=10KΩ

Therefore, $R_f = (A_v\text{-}1) \times R_1 = (11\text{-}1) \times 10 \times 10^3 = 100K\Omega$

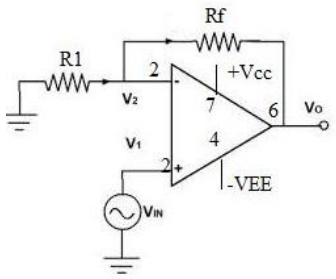


Fig. 2.3: Non-Inverting Amplifier

Procedure:-

1. Connect the circuit as per the circuit diagram shown in Fig.2.3
2. Apply sine wave as input with a magnitude of 1 V(p-p) and frequency 1 KHz.
3. Observe the output wave and note down the amplitude of output voltage.
4. Compare the practical value of V_o with its theoretical value.
5. Calculate the gain of the amplifier using $A_v = V_o / V_{in}$

Observations:

V_i = 1 V (p-p), f_i = 1 KHz

Sl. No.	Output voltage V_o (Volts) Practical	Output voltage V_o (Volts) Theoretical	Gain
1			

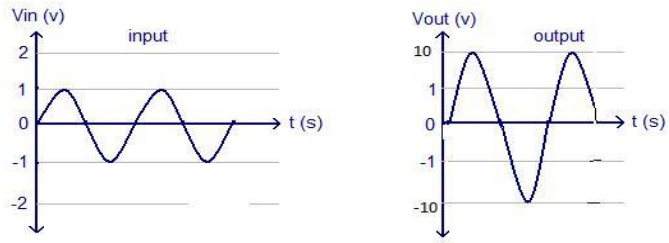


Fig. 2.4: Input and Output wave forms of Non- Inverting amplifier

Voltage Follower :-

If the feedback resistor, R*f* is made equal to zero, (R*f* = 0), and resistor R1 equal to infinity, (R1 = ∞), then the circuit would have a fixed gain of "1" as all the output voltage would be present on the inverting input terminal (negative feedback). This would then produce a special type of the non-inverting amplifier circuit called a **Voltage Follower**.

Voltage follower is an Op-amp circuit whose output voltage straight away follows the input voltage. That is output voltage is equivalent to the input voltage. Op-amp circuit does not provide any amplification. Thus, voltage gain is equal to 1. They are similar to discrete emitter follower.

The other names of voltage follower are Isolation Amplifier, Buffer Amplifier, and Unity-Gain Amplifier. The voltage follower provides no attenuation or no amplification but only buffering. This circuit has an advantageous characteristic of very high input impedance.

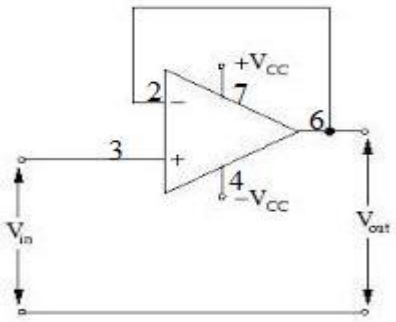


Fig. 2.5: Voltage Follower

Procedure:-

1. Connect the circuit as per the circuit diagram shown in Fig.2.5
2. Apply sine wave as input with a magnitude of 1 V(p-p) and frequency 1 KHz.
3. Observe the output wave and note down the amplitude of output voltage.
4. Compare the practical value of V_o with its theoretical value.
5. Calculate the gain of the amplifier using $A_v = V_o / V_{in}$

Observations:

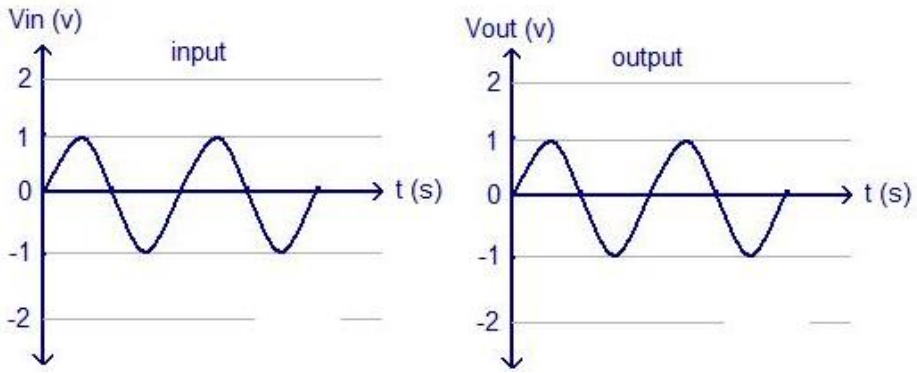


Fig. 2.5: Input and Output wave forms of Voltage follower

Result:

Studied the operation of the basic applications of op-amp and Gain of the Inverting amplifier, Non-Inverting amplifier and Voltage follower were determined.

Gain of the Inverting amplifier=…….

Gain of the Non-Inverting amplifier=……..

Gain of the Voltage follower=……..

Review Questions:

1. What is input bias current?
2. Why do we use R_{comp} resistor?
3. What is thermal drift?
4. Why is IC741 op-amp not used for high frequency applications?
5. What is unity gain circuit?
6. Which amplifier acts as a Subtractor?
7. Draw the circuit diagram of 3 input adder.
8. Draw an op- amp circuit whose output Vo is V1+ V2 – V3 –V4.

Experiment 3

Integrator and Differentiator Using Op-Amp

Aim :-

1. Design a differentiator to differentiate an input signal with fmax= 1 kHz.
2. Design an integrator circuit to properly process input waveform upto 1KHz.

Equipments/ Components Required:

Components:

Name	Specifications/ Range	Quantity
Op-amp	µA741C	1
Resistor	1KΩ, ¼ W	3
	1.5KΩ , ¼ W	2
	15KΩ, ¼ W	1
	10k, ¼ W	4
	150Ω, ¼ W	1
	100k, ¼ W	1
Capacitor	0.01uf	1
	0.1uf	1

Equipment

Name	Specifications/ Range	Quantity
IC Trainer board		1
Function generator	0-20MHz.	1
Dual trace CRO	0-200MHz	1
DC Power supply		1

Integrator:-

Operational amplifier can be configured to perform calculus operations such as differentiation and integration. In an integrating circuit, the output is the integration of the input voltage with respect to time.

A passive integrator is a circuit which does not use any active devices like op-amps or transistors.

An integrator circuit which consists of active devices is called an Active integrator. An active integrator provides a much lower output resistance and higher output voltage than is possible with a simple RC circuit.

Op-amp integrating circuit is inverting amplifier, with appropriately placed capacitor. Integrator circuits are usually designed to produce a triangular wave output from a square wave input.

Integrating circuits have frequency limitations while operating on sine wave input signals. The circuit in fig 3.1 is an integrator, which is also a low-pass filter with a time constant=R_1C. When a voltage, V_{in} is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit (voltage follower circuit) giving an overall gain of less than 1, thus resulting in zero output. As the feedback capacitor C begins to charge up, its reactance X_c decreases and the ratio of Z_f/R_1 increases producing an output voltage that continues to increase until the capacitor is fully charged. At this point the ratio of feedback capacitor to input resistor (Z_f/R_1) is infinite resulting in infinite gain and the output of the amplifier goes into saturation. (Saturation is when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with no control in between). The circuit design generate triangular wave providing square wave as input to the integrator. Hence, the integrator circuit generates integral output with respect to the input waveform.

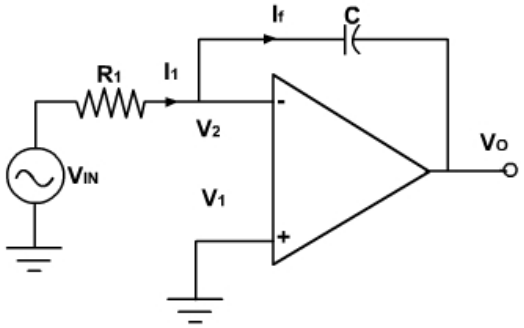


Fig.3.1: Integrator using Op-amp

Integrator has wide applications in Analog computers used for solving differential equations in simulation arrangements, A/D Converters, Signal wave shaping and Function Generators

Design of Integrator:-

The frequency responses of the practical and ideal integrator are shown in the above figure. For both circuits, the crossover frequency f_b, at which the gain is 0 dB, is given by:

$$f_b=1/2\pi R_1C_f$$

The 3 dB cut-off frequency f_a of the practical circuit is given by:

$$f_a=1/2\pi R_fC_f$$

Choose $f_b=10f_a$, $C_f=0.01\mu f$

We know that $f_b=1/2\pi R_1C_f$ =1KHz

Therefore, R1 = 15.9K ≈ 16KΩ

Now, $f_a= f_b/10$=100Hz

$f_a = 1/2\pi R_fC_f$ => **R_f =160KΩ**

Therefore, **R_{comp}= R1 ‖ Rf ≈ 15KΩ**

Circuit Diagram:

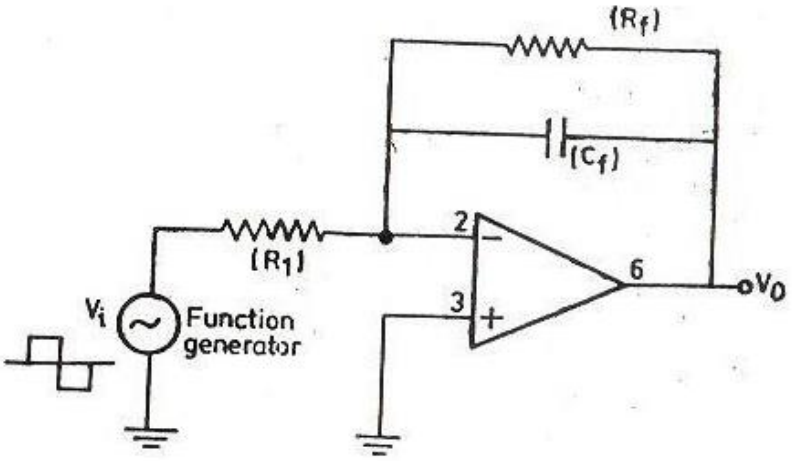


Fig.3.2: Integrator using Op-amp

Procedure (Integrator):-

1. Connect the circuit as per the circuit diagram shown Fig.3.2.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of V_{in} & V_o.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a triangular wave and note down the position, the amplitude and the time period of V_{in} & V_o.
8. Plot the output voltages corresponding to sine and square wave inputs.

Expected Waveforms Of Integrator:

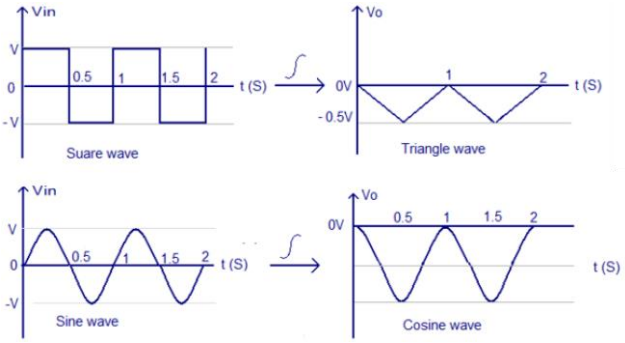


Fig.3.3: Expected Input and Output waveforms of Integrator

Differentiator:-

The basic Differentiator Amplifier circuit is the exact opposite to that of the Integrator operational amplifier circuit that we saw in the previous experiment. Here, the position of the capacitor and resistor have been reversed and now the Capacitor, C is connected to the input terminal of the inverting amplifier while the Resistor, R_1 forms the negative feedback element across the operational amplifier. This circuit performs the mathematical operation of Differentiation that is it produces a voltage output which is proportional to the input voltage's rate-of-change and the current flowing through the capacitor. Or in other words the output voltage is a scaled version of the derivative of the input voltage. The capacitor blocks any DC content only allowing AC type signals to pass through and whose frequency is dependent on the rate of change of the input signal. At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R_1/X_c) and low output voltage from the op-amp.

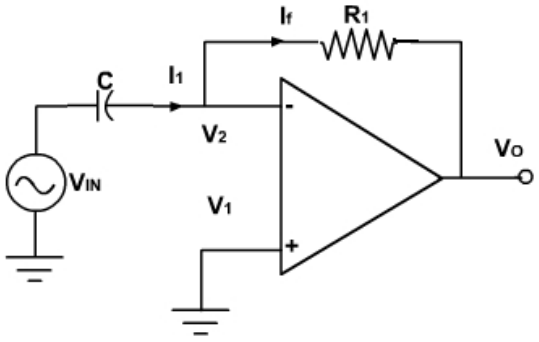


Fig.3.4: Differentiator using Op-amp

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$$V_o = - R_f C_1 \frac{dV_{in}}{dt}$$

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R_1 and C_f, **as shown in the circuit diagram**. This circuit is a practical differentiator. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to R_fC_1. That is, $T \geq R_fC_1$

Differentiator can be designed by implementing the following steps.

1. Select fa equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of C_1<1 μF, calculate the value of R_f

Calculate the values of $R_1$and C_f so that $R_1C_1=R_fC_f$.

Differentiator has wide applications in Monostable Multivibrator, Signal wave shaping and Function Generators.

Design:-

Given that f_b = fmax = 1 kHz

We know that $f_b = 1/2\pi R_1C_f$

Assuming $\mathbf{C_1 = 0.1\mu f}$, We get, $\mathbf{R_f = 1.5K\Omega}$

$f_a = 1/2\pi R_1C_1=10\mathbf{f}_b$

f_a=10KHz

R1=159Ω ≈ 150Ω

We know that $R_1C_1= R_fC_f$

Therefore, $\mathbf{C_f} = R_1C_1 / R_f$ **= 0.01μf**

Circuit Diagram:

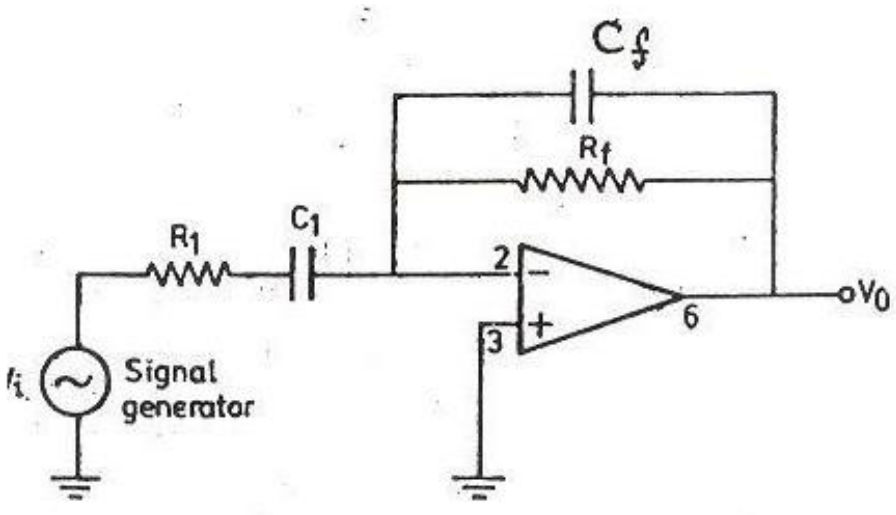


Fig.3.5: Differentiator using Op-amp

Procedure (Differentiator):-

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of Vin & Vo.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a spike wave and note down the position, the amplitude and the time period of Vin & Vo.
8. Plot the output voltages corresponding to sine and square wave inputs.

EXPECTED WAVEFORMS OF DIFFERENTIATOR:--

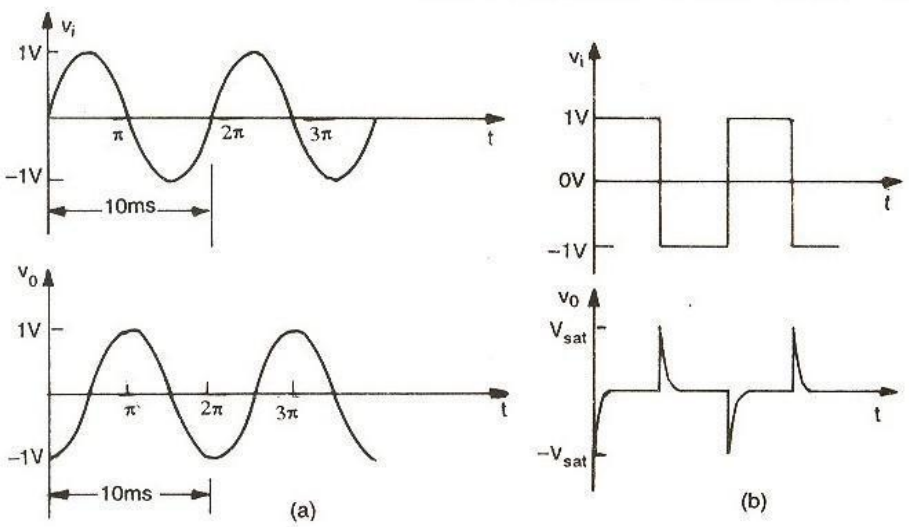


Fig.3.6: Expected Input and Output waveforms of Differentiator

Result:-

Review Questions:-

1. What is an Integrator?
2. Draw the circuit of the Integrator using op-amp IC741.
3. Write down the expression for Vo of an Integrator.
4. Draw the frequency response of the Integrator and explain.
5. Draw the output waveform of the Integrator when the input is a Square wave.
6. What is the purpose behind the connection of Rf in the feedback path of Integrator?

7. What are the applications of Integrator?
8. Why R_{comp} is used in both Integrator and Differentiator circuits?
9. What is a Differentiator?
10. Draw the circuit of the Differentiator using op-amp IC741.
11. Write down the expression for V_o of a Differentiator.
12. Draw the output waveform of the Differentiator when the input is a Sine wave.
13. Why R1 and Cf are connected in the circuit of the Differentiator?
14. What are the applications of Differentiator?

Experiment 4

ACTIVE FILTERS

Aim:- To design a first order low pass, high pass filter at a cut off frequency of 1KHz with a pass band gain at 2.

To design a first order Butterworth narrow band pass filter at a cut off frequency of 10 KHz with Q=10.

Equipments/ Components Required:

Components:

Name	Specifications/ Range	Quantity
Op-amp	μA741C	1
Resistor	15KΩ	1
	1KΩ	1
	10kΩ	3
	100Ω	1
Capacitor	-0.01uf,1nf	1

Equipments:

Name	Specifications/ Range	Quantity
IC Trainer board	---	1
Function generator	0-20MHz.	1
Dual trace CRO	0-200MHz	1
DC Power supply		

Theory:-

In the RC Passive Filter, a basic first-order filter circuits, such as the low pass and the high pass filters, can be made using just a single resistor in series with a non-polarized capacitor connected across a sinusoidal input signal.

It is also noticed that the main disadvantage of passive filters is that the amplitude of the output signal is less than that of the input signal, ie, the gain is never greater than unity and that the load impedance affects the filters characteristics.

With passive filter circuits containing multiple stages, this loss in signal amplitude called "Attenuation" can become quiet severe. One way of restoring or controlling this loss of signal is by using amplification through the use of **Active Filters**.

As their name implies, **Active Filters** contain active components such as operational amplifiers, transistors or FET's within their circuit design. They draw their power from an external power source and use it to boost or amplify the output signal.

Filter amplification can also be used to either shape or alter the frequency response of the filter circuit by producing a more selective output response, making the output bandwidth of the filter narrower or even wider. Then the main difference between a "passive filter" and an "active filter" is amplification.

An active filter generally uses an operational amplifier (op-amp) within its design and in the Operational Amplifier tutorial we saw that an Op-amp has high input impedance, a low output impedance and a voltage gain determined by the resistor network within its feedback loop.

Unlike a passive high pass filter which has in theory an infinite high frequency response, the maximum frequency response of an active filter is limited to the Gain/Bandwidth product (or open loop gain) of the operational amplifier being used. Still, active filters are generally much easier to design than passive filters, they produce good performance characteristics, very good accuracy with a steep roll-off and low noise when used with a good circuit design.

Active Low Pass Filter

The most common and easily understood active filter is the **Active Low Pass Filter**. Its principle of operation and frequency response is exactly the same as those for the previously seen passive filter, the only difference this time is that it uses an op-amp for amplification and gain control. The simplest form of a low pass active filter is to connect an inverting or non-inverting amplifier, the same as those discussed in the Op-amp tutorial, to the basic RC low pass filter circuit as shown.

This first-order low pass active filter consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer) giving it a DC gain of one, Av = +1 or unity gain as opposed to the passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

While this configuration provides good stability to the filter, its main disadvantage is that it has no voltage gain above one. However, although the voltage gain is unity the power gain is very high as its output impedance is much lower than its input impedance. If a voltage gain greater than one is required we can use the following filter circuit.

These Active Filters are most extensively used in the field of communications and signal processing. They are employed in one form or another in almost all sophisticated electronic systems such as Radio, Television, Telephone, Radar, Space Satellites, and Bio-Medical

Equipment. Active Filters employ transistors or Op – Amps in addition to that of resistors and capacitors. Active filters have the following advantages over passive filters. (1) Flexible gain and frequency adjustment. (2) No loading problem (because of high input impedance and low output impedance) and (3) Active filters are more economical than passive filters.

Design of First Order Low Pass Filter:-

Cut off frequency is given as f_c=1 kHz

Assume that C=0.01uf

Therefore, **R** = 1 / $2\pi f_c C$ **=16KΩ**

Given that Pass band gain, A = 2

We know that A = 1 + R_f / R_1

Therefore, 2 = 1 + R_f / R_1

Therefore, **R_f = R_1 = 10KΩ**

Circuit Diagram of First Order Low Pass Filter:-

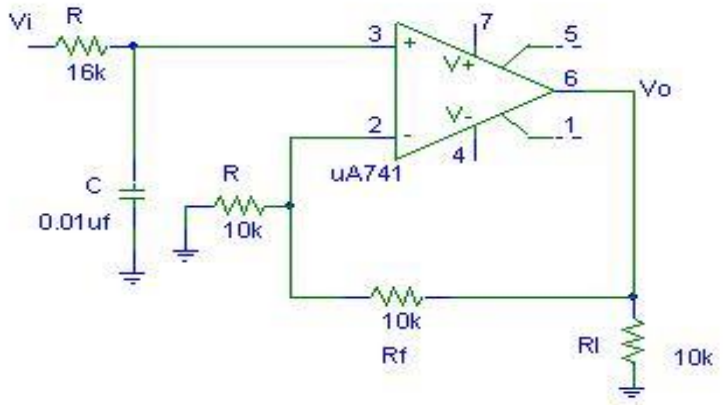


Fig.4.1: First Order Low Pass Filter

Expected Plot of Frequency Response:-

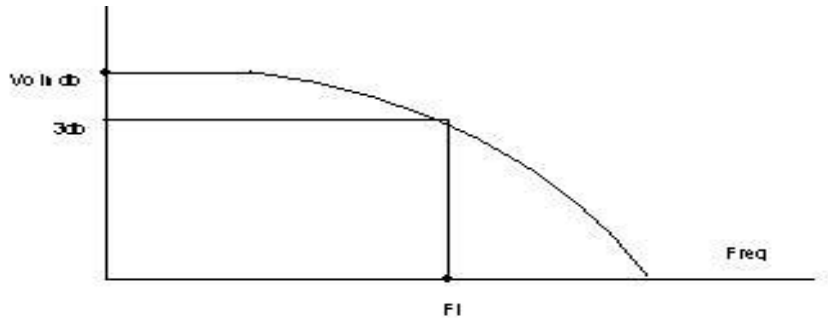


Fig. 4.2: Expected plot of Frequency Response of First order Low Pass Filter

First Order High Pass Filter:-

The basic operation of an **Active High Pass Filter** (HPF) is the same as RC passive high pass filter circuit, except an operational amplifier or included within its design providing amplification and gain control.

Like the active low pass filter circuit, the simplest form of an *active high pass filter* is to connect a standard inverting or non-inverting operational amplifier to the basic RC high pass passive filter circuit as shown in Fig.4.3.

First Order High Pass Filter

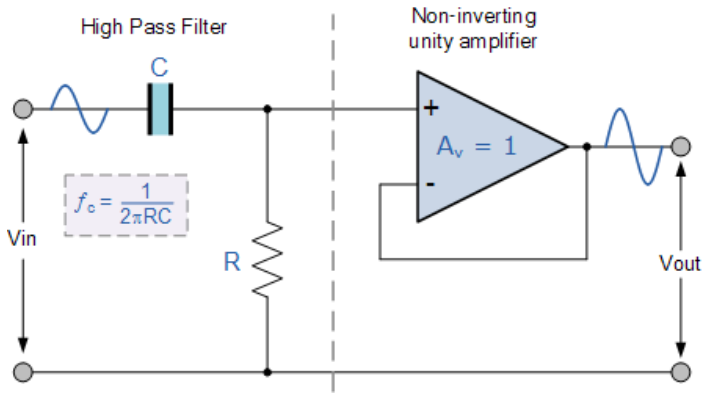


Fig.4.3: First Order High Pass Filter

Technically, there is no such thing as an **active high pass filter**. Unlike Passive High Pass Filters which have an "infinite" frequency response, the maximum pass band frequency response of an active high pass filter is limited by the open-loop characteristics or bandwidth of the operational amplifier being used, making them appear as if they are band pass filters with a high frequency cut-off determined by the selection of op-amp and gain.

In the Operational Amplifier tutorial we saw that the maximum frequency response of an op-amp is limited to the Gain/Bandwidth product or open loop voltage gain (A_V) of the operational amplifier being used giving it a bandwidth limitation, where the closed loop response of the op amp intersects the open loop response.

A commonly available operational amplifier such as the uA741 has a typical "open-loop" (without any feedback) DC voltage gain of about 100dB maximum reducing at a roll off rate of -20dB/Decade (-6db/Octave) as the input frequency increases. The gain of the uA741 reduces until it reaches unity gain, (0dB) or its "transition frequency" (ft) which is about 1MHz. This causes the op-amp to have a frequency response curve very similar to that of a first-order low pass filter and this is shown in Fig. .

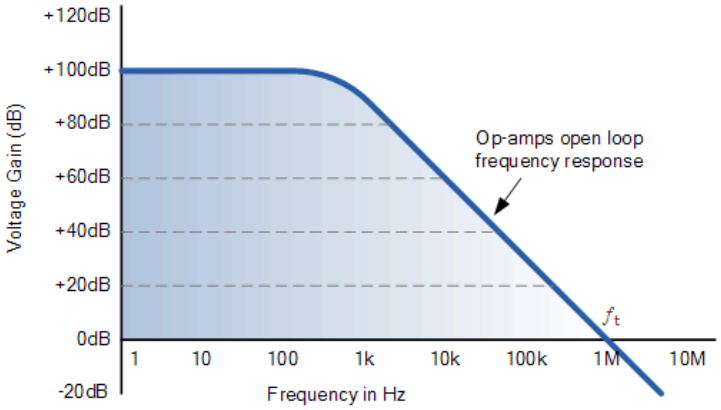


Fig.4.4: Frequency Response Of First Order High Pass Filer

Active High Pass Filter

A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuates low frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

Design of First Order High Pass Filter

Given that Cut off frequency, f_c =1 kHz

Assuming **C=0.01µF**, Therefore **R**= $1/2\pi f_c C$ **= 16KΩ**

Given that Pass band gain, A = 2

We know that Pass band gain, A=1 + R_f / R_1

Therefore, 2 = 1+ R_f /R_1

Therefore, **R_f = R_1 = 10KΩ**

Circuit Diagram of First Order High Pass Filter:-

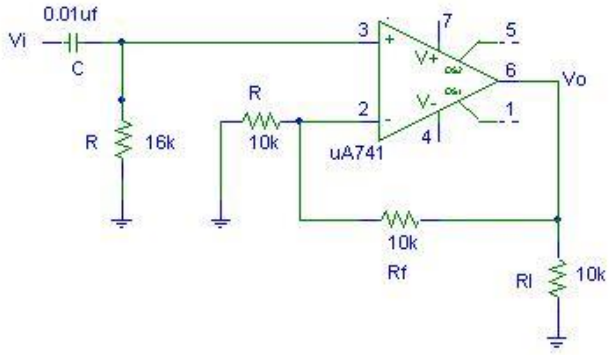


Fig.4.5: Circuit Diagram Of First Order High Pass Filter

Expected Plot of Frequency Response Of First Order High Pass Filter:-

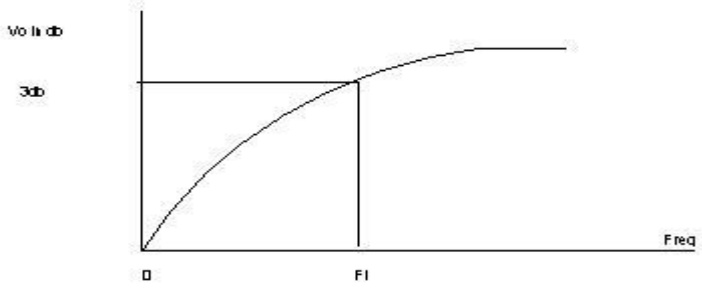


Fig.4.6: Frequency Response Of First Order High Pass Filter

Design of Narrow Band Pass Filter:-

Given that Pass Band gain, A = 10, f_c=10 KHz and Q=10

Assuming that C=0.01μF, $R_1 = Q/2\pi fc.C.A = 1.6\ K\Omega$

$$R_2 = Q / 2\pi\ fc.\ C.\ (2Q^2-A) = 100\Omega$$

$$R3 = Q / 2\pi\ fc.\ C = 32K\Omega$$

Circuit Diagram of Narrow Band Pass Filter:-

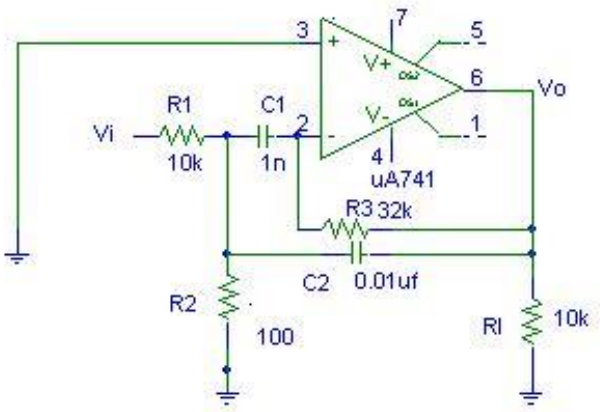


Fig.4.7:Circuit Diagram Of Narrow Band Pass Filter

Procedure:-

1. Connect the circuit as shown in figure.
2. Adjust V_{in} = 4v (P-P) & keep it constant thought-out the experiment.
3. Vary the input frequency from 20Hz to 20 KHz & Note down peak to peak voltage across R_l using CRO.
4. Plot variations of voltage gain v/s frequency on semilog graph & find 3 db frequencies.

Observations & Calculations:

V_{in} = 4v (P-P)			
Frequency(Hz)	**Input Voltage(V)**	**Output Voltage(V)**	**Gain**
100			
500			
800			
1K			
1.5K			
2K			
8K			
15K			
20K			
30K			
50K			

Expected Plot of Frequency Response:-

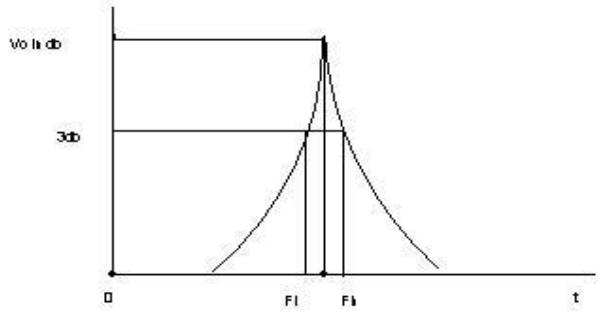


Fig. : Frequency Response of Narrow Band Pass Filter

Result:- The filters are designed to give specifications & their frequency response is plotted as shown.

Review Questions:-

1. How filters are classified? Give one example for each classification.
2. What is an active filter and why it is called so?
3. How an active filter differs from a passive filter?
4. What are the advantages of active filters over passive filters?
5. Draw the circuit diagrams of active filters LPF and HPF.
6. Draw the frequency response of all filters (LPF, HPF, BPF, BRF and All-pass).
7. What is the gain roll off rate for a 1st order and 2nd order filter?
8. What is the formula for cut-off frequency?
9. What is a 3 dB frequency and why it is called so?
10. What are the other names for 3 dB frequency?

Experiment 5

TRIANGULAR WAVE GENERATOR USING OP-AMP

Aim: - To design a Triangular wave generator of 1KHz using µA741 op-amp with Vpp = 5V, VCC=+15v, VEE= -15V and to determine the threshold voltage V_{UT} & V_{LT}.

Equipments / Components Required:-

Components:

Name	Specifications / Range	Quantity
Op-amp	µA741	1
Resistor	56KΩ, ¼ W	1
	139KΩ, ¼ W	1
	10kΩ, ¼ W	1
Capacitor	0.01µf	1

Equipments:

Name	Specifications / Range	Quantity
IC Trainer board		1
Dual trace CRO	0-200MHz	1
DC Power supply		

Theory:-

Triangular wave is a periodic, non-sinusoidal waveform with a triangular shape. People often get confused between triangle and sawtooth waves. The most important feature of a triangular wave is that it has equal rise and fall times while a sawtooth wave has un-equal rise and fall times. The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc. There are many methods for generating triangular waves but here we focus on method using opamps. This circuit is based on the fact that a square wave on integration gives a triangular wave.

The circuit uses an opamp based square wave generator for producing the square wave and an op- amp based integrator for integrating the square wave. The circuit diagram is shown in the Fig.5.1.

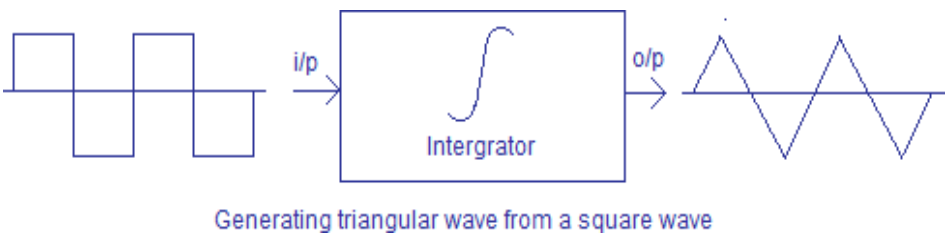


Fig.5.1: Generation of Triangular Waveform from Square Wave

Design:-

Given that f_o = 1KHz, V_{pp} = 2V, V_{CC} = -V_{EE} = 15V, ±Vsat = 14V, R_2=10KΩ, C_1 = 0.01µF

We know that $V_{pp} = 2R_2 / R_3.V_{sat}$

Therefore, $R_3 = 2\ R_2.V_{sat} / V_{pp}$ = 56 KΩ (Use 100KΩ Potentiometer)

We know that $f_o = R_3 / (4R_1C_1R_2)$.

Therefore, R_1 = 140KΩ

Circuit Diagram:-

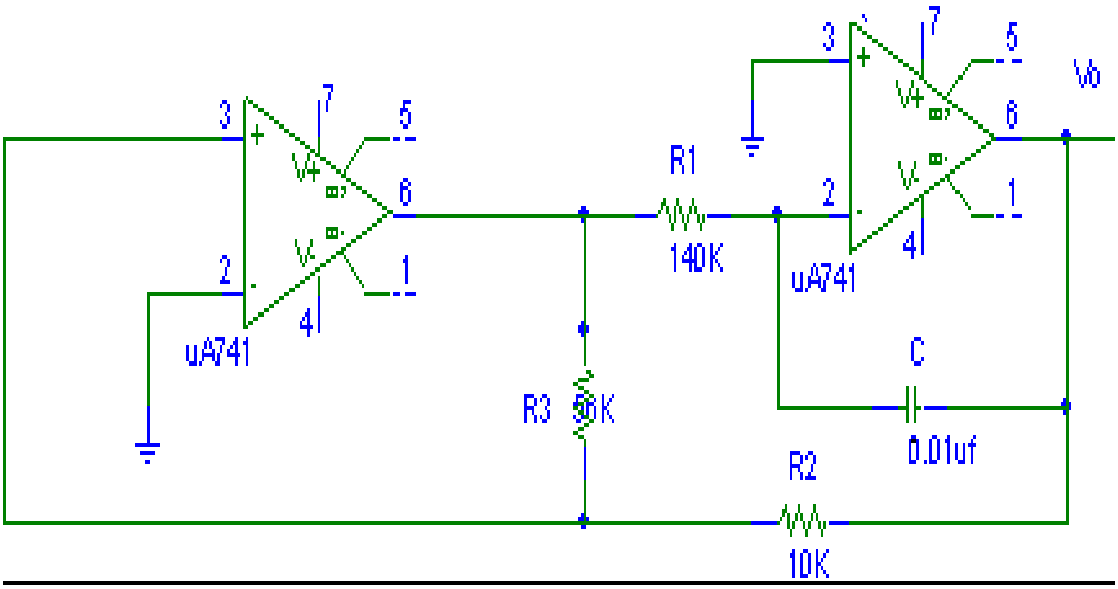


Fig.5.2: Triangular Wave Generator Using Op-Amp

Procedure:-

1. The connections are made as per the circuit diagram as shown in Fig.5.2.
2. Observe the Square waveform (a) The output of A1 & Triangular waveform (b) the output A2.
3. Observe the hysteresis curve & Note down the values for the V_{UT}&V_{LT} & hence V_H (Hysteresis curve).

Observations:-

+Vsat= -Vsat=

+Vramp= -Vramp=

V_{UT}= V_{LT}=

Vh=

Time period of the triangular wave =

Expected Plot of Input and Output Waveforms And Hysteresis

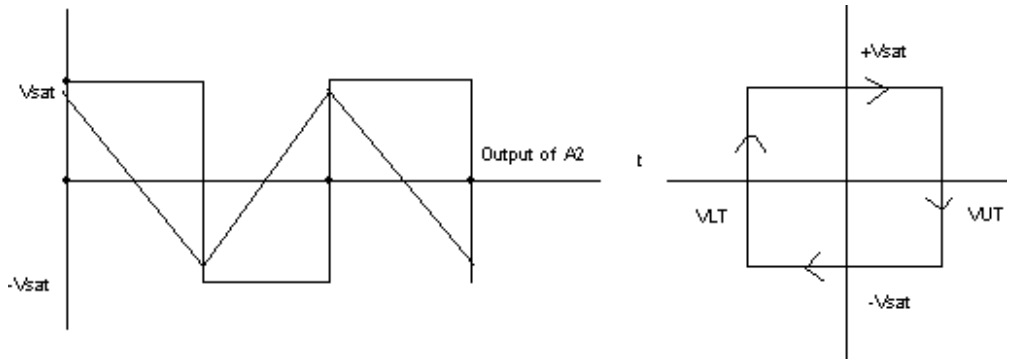


Fig.5.3: Input and Output Waveforms and hysteresis

Experiment -6

ASTABLE MULTIVIBRATOR USING 555 TIMER

Aim:-To design an Astable multivibrator using 555 timer & to generate q square wave of 75% duty cycle & amplitude 5V, frequency of 1 KHz.

Equipments/ Components Required:-

Components:

Name of the Component	Specifications / Range	Quantity
IC 555	---	1
Resistor	7.2KΩ	1
	3.2KΩ	1
Capacitor	0.01µf	1
	0.1µf	2

Equipments:

Name of the Equipment	Specifications/ Range	Quantity
IC Trainer Board		1
Function Generator	0 - 20 MHz	1
DC Power Supply		1

Theory:-

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave generating circuit. Unlike the monostable multivibrator this circuit does not require any external triggering to change the state of the output, hence the name free-running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer.

Astable operation: Initially when output is high, capacitor C starts charging toward Vcc through RA and RB. However as soon as voltage across the capacitor equals 2/3 Vcc, the comparator 1 triggers the flip-flop and the output switches to low. Now capacitor C stars discharging through RB and transistor Q1. When the voltage across C equals 1/3 Vcc, comparator 2"s output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage and capacitor voltage are shown IN GRAPHS.

As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 Vcc, respectively. The time during which the capacitor charge from 1/3 Vcc to 2/3 Vcc is equal to the time the output is high and is given by

$tc = 0.69(R_A + R_B)\ C$ ……..(a)

Where R_A and R_B are in ohms and C is in farads.

Similarly, the time during which the capacitor discharges from 2/3Vcc to 1/3Vcc is equal to the time the output is low and is given by

$td = 0.69(R_A)\ C$ …….. (b)

Thus the total period of output waveform is

$T = tc + td = 0.69(R_A + 2R_B)\ C$ …….. (c)

Frequency of Oscillation is

$fo = 1/T = .\ 1.45 / (R_A + 2R_B)\ C$ …….. (d)

Duty Cycle:- The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

$\%$ duty cycle $= (\ tc\ /T)\times 100 = ((R_A + R_B)\ /(R_A + 2R_B))X100$ …….(e)

Design Of Astable Multivibrator Using 555 Timer:-

Given that duty cycle = 75%, frequency =1 KHz

We know that $f = 1.45 / (R_A+2R_B)\ C$

Assume that C = 0.1µF, Therefore, $R_A + 2R_B = 1.45 / 0.1*10^{-6} *1x\ 10^3 = 1.45\ K\Omega$

We know that the duty cycle is given by $D = R_B / (R_A+2R_B) = 75/100$

Therefore, $4R_B = R_A + 2\ R_B$, which implies $R_A = 2R_B$

However, $R_A + 2R_B = 1.45\ k\Omega$

Therefore, $4R_B = 14.5\ K\Omega$

Therefore, $R_B = 36.25\ K\ \Omega \approx 3.7K\Omega$ and $R_A = 14.5K\Omega - 2R_B = 7.2K\Omega$

Circuit Diagram:-

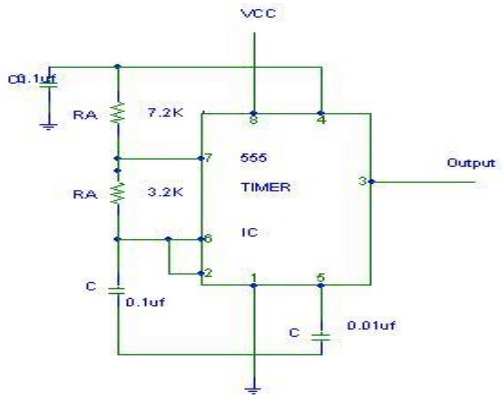


Fig. 6.1:Astable Multivibrator using IC 555

Procedure:-

1. The connections are made as per the circuit diagram shown in Fig. 6.1.
2. Observe the output wave form (a). pin3 & Compare it with theoretical value.
3. Also observe the waveform (a) pin6 (across c) & check that amplitude should by 2/3 VCC.

Observations:-

T_{low}=0.7*0.5ms

T_{high}=1.9*0.5ms=0.95ms

$T=T_{low}+T_{high}$=1.3ms

Duty cycle=0.35ms/1.3,ms=26.9%

Expected Output Wave Forms:-

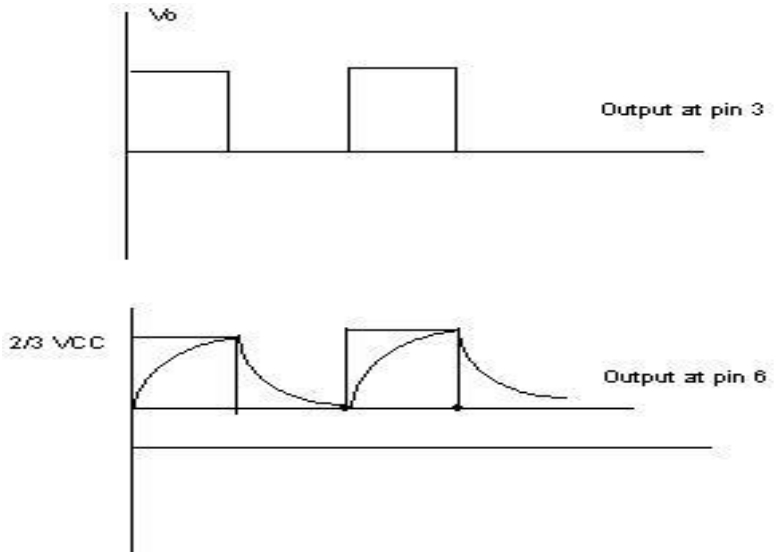


Fig. 6.2 Expected Output Waveforms

Result:- An Astable multivibrator is designed using 555 timer which generates a square wave.

MONOSTABLE MULTIVIBRATOR USING 555 TIMER

Aim:- To design a monostable multivibrator using 555 timer to generate a pulse width of 1msec & amplitude of 5V for each trigger input.

Equipments/ Components Required:-

Components:

Name	Specifications/ Range	Quantity
Timer IC	IC 555	1
Diode	DA9A	1
Resistor	10KΩ, ¼ W	1
Capacitor	0.01µf	1
	0.1µf	1
	10µf	1

Equipment:

Name	Specifications/ Range	Quantity
IC Trainer board		1
Function generator	0-20MHz.	1
DC Power supply		

Theory:- A monostable multivibrator, often called a one-shot multivibrator, is a Pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go high ($\cong V_{cc}$). The time the output remains high is determined by the external RC network connected to the timer. AT the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output remains low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low), hence the name monostable. Normally, the output of the monostable multivibrator is low.

Monostable operation: Initially when output is low, that is, the circuit is in a stable state, transistor Q_1 is on and the capacitor C is shorted out of the ground. However, upon application of a negative trigger pulse to pin 2, transistor Q_1 is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward V_{cc} through R_A. However, when the voltage across the capacitor equals 2/3 V_{cc}, comparator 1‟s output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-

flop turns transistor Q1 ON, and hence capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Fig.(c) shows the trigger input, output voltage, and capacitor voltage waveform. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 V_{cc}. The time duration that the output remains high is given by $t_p = 1.1R_AC$ seconds

Design Of Monostable Multivibrator Using 555 Timer:-

Given that t_p = 1msec

Choose C = 0.1 µF

We know that $t_p = 1.1R_AC$

Therefore, $R_A = 1x10^3 / (1.1x\ 0.1\ x\ 10^{-6}) = 10K\Omega$

Also, $R_1 = (0.01\ x\ 10^{-3}) / (0.01\ x\ 10^{-6}) = 1K\Omega$

Hence, the designed components are C = 0.1µF, C_1 = 0.01µF, R_1 = 1KΩ, R_A = 10KΩ

Circuit Diagram:-

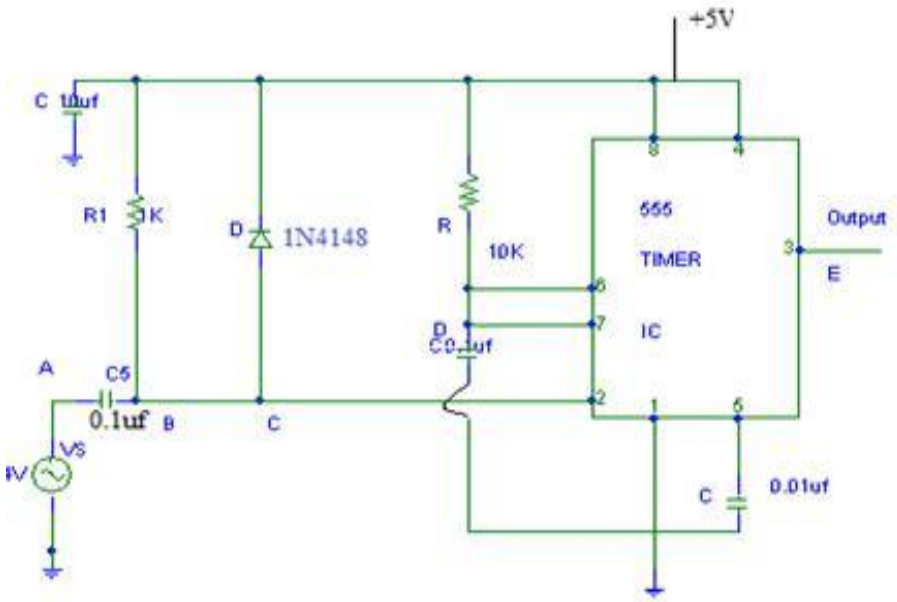


Fig.6.3:Monostable Multivibrator Using 555 Timer

Procedure:-

1. Connections are made as per the circuit diagram]
2. Apply input trigger voltage at pin2 of 555 timer IC
3. Note down the waveforms at A, B, C, D, &E.
4. Measure the pulse width of the output waveforms at pin 3.

Expected Plot of Waveforms:-

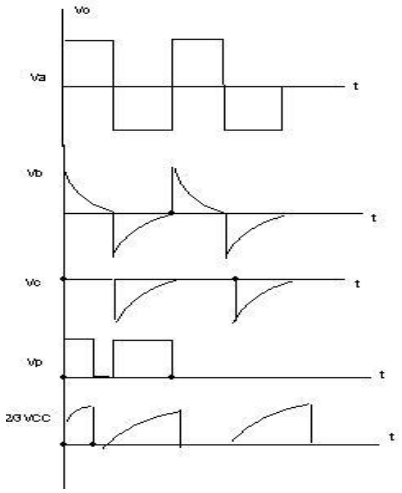


Fig.6.4: Expected Waveforms

RESULT:- A Monostable multivibrator is designed using 555 timer which generates a pulse width

REVIEW QUESTIONS:-

1. What is the other name for monostable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV?
4. Which type of trigger pulse is required for MSMV?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?
7. Explain the functional block diagram of a 555 timer
8. Explain the function of reset.
9. What are the modes of operation of timer?
10. What is the expression of time delay of a monostable multivibrator?
11. Discuss some applications of timer in monostable mode.
12. Define duty cycle
13. **Give** methods of obtaining symmetrical waveform.
14. How is a monostable multivibrator connected into a pulse position modulator?
15. How Schmitt trigger circuit is constructed using 555 timer?
16. Draw the pin diagram of 555 timer.

PART-B

Experiment -7

Flip Flop conversions and latches using gates and ICs.

Aim:-

1. To verify the truth table of RS Latch and D Latch.
2. To verify the truth table of JK Flip Flop using Gates and IC 7476.
3. To realize D & T flip flop using JK flip flop of IC 7476.

Equipments/ Components Required:-

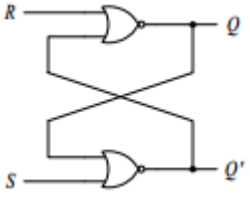
Name	Specifications/ Range	Quantity
IC	7400	1
	7402	1
	7404	1
	7411	1
Digital IC Trainer Kit		1

Theory:-

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

SR LATCH:-

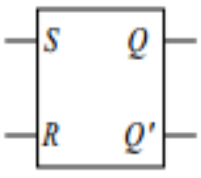
A bistable multivibrator has *two* stable states, as indicated by the prefix *bi* in its name. Typically, one state is referred to as *set* and the other as *reset*. The simplest bistable device, therefore, is known as a *set-reset*, or S-R, latch. To create an S-R latch, we can wire two NOR gates in such a way that the output of one feeds back to the input of another, and vice versa, like this:



Logic Diagram

S	R	Q	Q_{next}	Q_{next}'
0	0	0	0	1
0	0	1	1	0
0	1	×	0	1
1	0	×	1	0
1	1	×	0	0

Truth Table



Symbol

Fig.7.1: SR Latch

Procedure:-

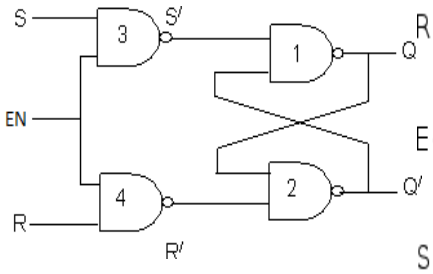
1. Connect the logic diagram as shown in Fig. 7.1
2. Verify the truth table of SR Latch

THE GATED S-R LATCH:-

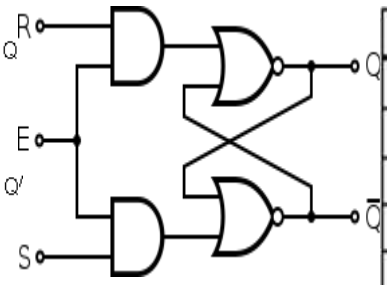
When the E=0, the outputs of the two AND gates are forced to 0, regardless of the states of either S or R. Consequently, the circuit behaves as though S and R were both 0, latching the Q and not-Q outputs in their last states.

Only when the enable input is activated (1) will the latch respond to the S and R inputs.

It is sometimes useful in logic circuits to have a multivibrator which changes state only when certain conditions are met, regardless of its S and R input states. The conditional input is called the *enable*, and is symbolized by the letter E.



Using NAND



Using NOR

Logic Diagram

E	S	R	Q	Q_{next}	Q_{next}'
0	x	x	0	0	1
0	x	x	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	x	0	1
1	1	0	x	1	0
1	1	1	x	1	1

Truth Table

Fig.7.2: SR Latch With Enable Input

Procedure:-

1. Connect the logic diagram as shown in Fig. 7.2
2. Verify the truth table of SR Latch with enable input

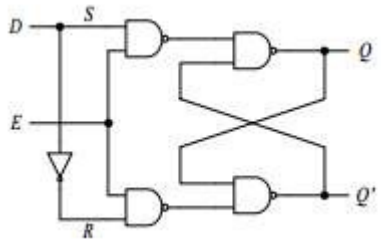
D LATCH:-

Since the enable input on a gated S-R latch provides a way to latch the Q and not-Q outputs without regard to the status of S or R, we can eliminate one of those inputs to create a multivibrator latch circuit with no "illegal" input states. Such a circuit is called a D latch, and its internal logic looks like this.

Note that the R input has been replaced with the complement (inversion) of the old S input, and the S input has been renamed to D. As with the gated S-R latch, the D latch will not

respond to a signal input if the enable input is 0—it simply stays latched in its last state. When the enable input is 1, however, the Q output follows the D input

Since the R input of the S-R circuitry has been done away with, this latch has no "invalid" or "illegal" state. Q and not-Q are *always* opposite of one another.



E	D	Q	Q_{next}	Q_{next}'
0	×	0	0	1
0	×	1	1	0
1	0	×	0	1
1	1	×	1	0

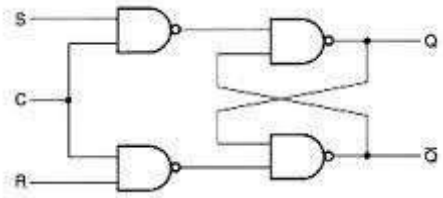
Logic Diagram **Truth Table**

Fig.7.3: D Latch

Procedure:-

1. Connect the logic diagram as shown in Fig. 7.3
2. Verify the truth table of D Latch

SR FLIPFLOP:-



C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

Logic Diagram **Truth Table**

Fig.7.4: SR Flip-flop

Procedure:-

1. Connect the logic diagram as shown in Fig. 7.4
2. Verify the truth table of SR Flip-flop

JK FLIPFLOP:-

Another variation on a theme of bistable multivibrators is the J-K flip-flop. Essentially, this is a modified version of an S-R flip-flop with no "invalid" or "illegal" output state.

What used to be the S and R inputs are now called the J and K inputs, respectively. The old two-input AND gates have been replaced with 3-input AND gates, and the third input of each gate receives feedback from the Q and not-Q outputs.

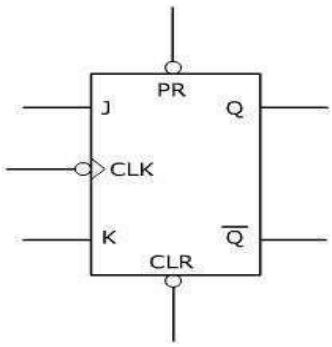
What this does for us is permit the J input to have effect only when the circuit is reset, and permit the K input to have effect only when the circuit is set.

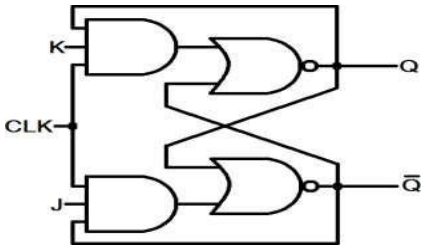
In other words, the two inputs are *interlocked*, to use a relay logic term, so that they cannot both be activated simultaneously.

If the circuit is "set," the J input is inhibited by the 0 status of not-Q through the lower AND gate; if the circuit is "reset," the K input is inhibited by the 0 status of Q through the upper AND gate.

When both J and K inputs are 1, however, something unique happens. Because of the selective inhibiting action of those 3-input AND gates, a "set" state inhibits input J so that the flip-flop acts as if J=0 while K=1 when in fact both are 1.

On the next clock pulse, the outputs will switch ("toggle") from set (Q=1 and not-Q=0) to reset (Q=0 and not-Q=1). Conversely, a "reset" state inhibits input K so that the flip-flop acts as if J=1 and K=0 when in fact both are 1. The next clock pulse toggles the circuit again from reset to set.





CLOCK	J	K	$\overline{PRESET}$	$\overline{RESET}$	Q	$\overline{Q}$
.	.	.	0	1	1	0
.	.	.	1	0	0	1
↓	0	0	1	1	Q	$\overline{Q}$
↓	1	0	1	1	1	0
↓	0	1	1	1	0	1
↓	1	1	1	1	$\overline{Q}$	Q

Symbol **Logic Diagram** **Truth Table**

Fig. 7.5. : JK Flip- Flop

Procedure:-

1. Connect the logic diagram as shown in Fig. 7.5
2. Verify the truth table of JK Flip-flop

Realisation of D & T Flip Flop using JK Flip Flop IC 7476:-

JK Flip-flop IC 7476: The **SN7476** is a **dual in-line JK flip flop IC**, i.e. it has two JK flip flops inside it and each can be used individually based on our application. The term JK flip flop comes after its inventor Jack Kilby. The JK flip flops are considered to be the most efficient flip-flop and can be used for certain applications on its own. The flip-flops are also called as latching devices meaning it can remember one single bit of data and latch the output based on it, due to this property they are commonly used as shift registers, control registers, storage registers or where ever a small memory is required. More than one Flip Flop can be used in series to act as an EEPROM for holding small amount of data. The JK flip flop is

considered to be more suitable for practical application because of its truth table that is the output of the flip flop will be stable for all types of inputs.

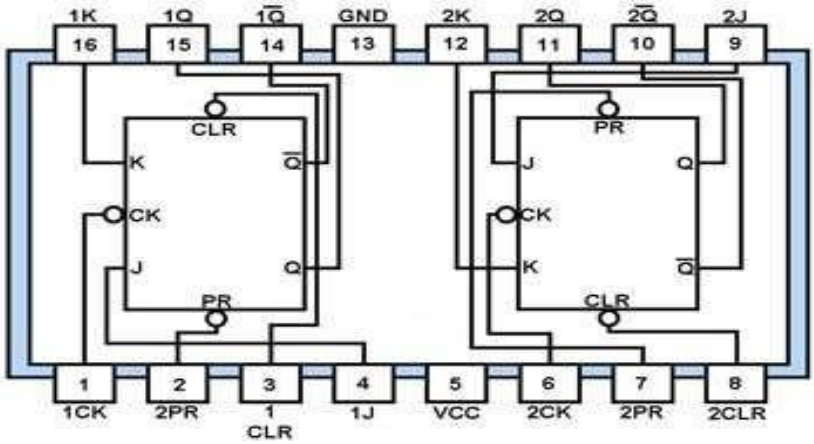


Fig. 7.6: SN7476 (dual in-line JK flip flop IC)

D Flip-flop using JK Flip-flop:

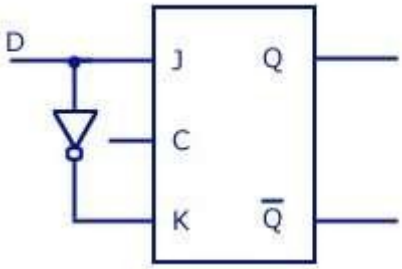


Fig.7.7: Logic Diagram of D-FF using JK FF

T Flip-Flop using JK Flip-Flop:

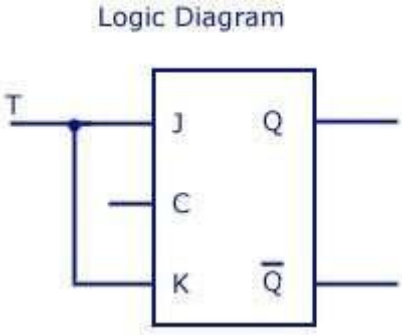


Fig.7.8: Logic Diagram of T Flip-Flop using JK Flip-flop

PROCEDURE:-

1. Connect the circuit and verify the truth tables of all flip-flops.

RESULT:-Latches and flip flops have been verified and realization of D and T flip flop using JK Flip Flop is done successfully**.**

Experiment -8

SYNCHRONOUS AND ASYNCRONOUS COUNTERS

Aim:-

1. To design 3 bit ripple counter
2. To design & Realize mod -5 Ripple counter (CLK=1 kHz)
3. To design & Realize mod -5 synchronous counter (CLK=1 kHz) by skipping 010,100,110 states. (Use JK flip-flop)
4. To obtain the count sequence in IC 7490 when the output Q2 is connected to input A and pulse are applied at input B.

Equipments/ Components Required:-

Name	Specifications/ Range	Quantity
IC	7476	1
	7408	1
Trainer Kit	---	1

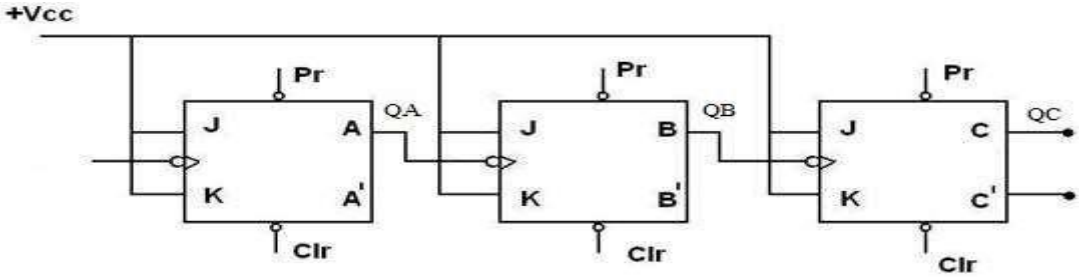
Theory:-

A counter is a sequential circuit that counts in a cyclic sequence. It is essentially a register that goes through a predetermined sequence of states upon the application of input pulses. There are two types of counters – Synchronous Counter & Asynchronous Counter. In a synchronous counter, the input pulses are applied to all clock pulse inputs of all flip flops simultaneously (directly). Synchronous counter is also known as **parallel sequential circuit**. Examples of Synchronous Counters are Ring Counter and Johnson Counter (Switch Tail or Twisted Ring Counter)

In an asynchronous counter, the flip flop output transition serves as a source for triggering other flip flops. In other words, the clock pulse inputs of all flip flops, except the first, are triggered not by the incoming pulses, but rather by the transition that occurs in previous flipflop‟s output.. Asynchronous counter is also known as **serial sequential circuit**. Example of Asynchronous Counters is Binary Ripple Counter and Up Down Counter. Synchronous counters are faster than asynchronous counter because in synchronous counter all flip flops are clocked simultaneously.

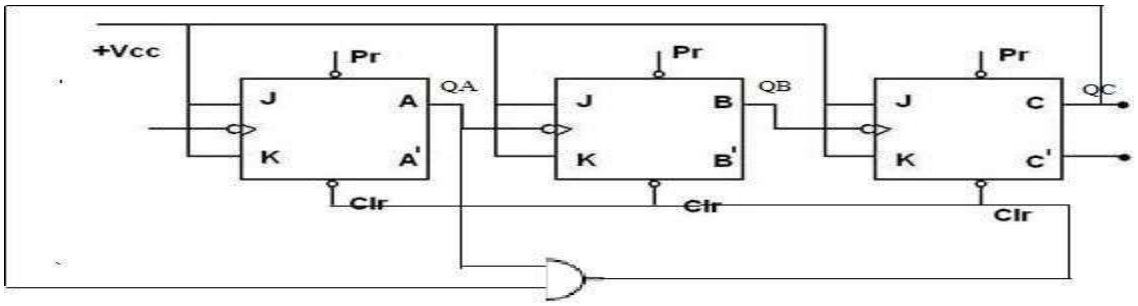
Circuit Diagrams:-

1. 3 Bit Ripple Counter



2. Mod 5 Ripple Counter

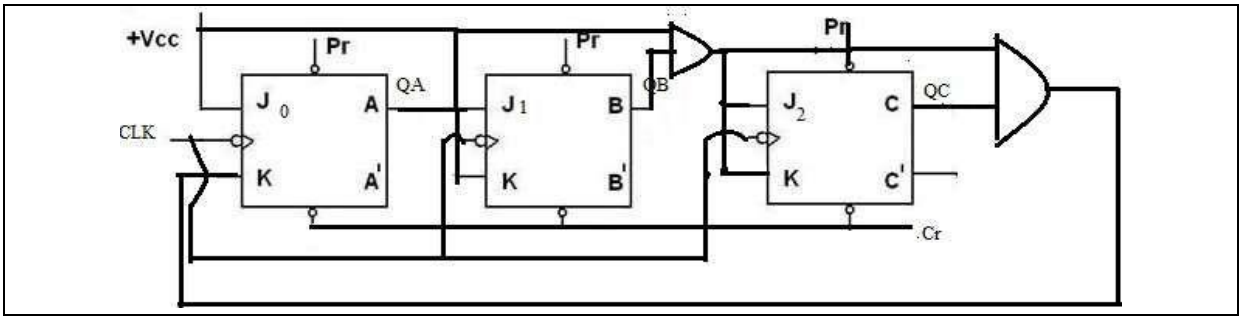
A counter which is reset at the fifth clock pulse is called Mod 5 counter or Divide by 5 counter. The circuit diagram of Mod 5 counter is shown in the figure. This counter contains three JK flip- flop.



3. Mod 5 Synchronous Counter

Q2	Q1	Q0	J0 K0		J1	K1	J2 K2	
0	0	0	1	X	0	X	0	X
0	0	1	X	0	1	X	0	X
0	1	1	X	0	X	1	1	X
1	0	1	X	0	1	X	X	0
1	1	1	X	1	1	X	X	1
0	0	0						

On simplification by using K-map J0 =1; J1=QA; J2= QBQA; K0=QCQBQA; K1=1; K2= QBQA;



4. IC 7490 Decade Counter

S no	Q3Q2Q1Q0			
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
	0	0	0	0

RESULT:-

REVIEW QUESTIONS:-

1. What is decade counter?
2. How to design modulo-10 counter?
3. What is up-down counter?
4. What is a sequential circuit?
5. Differentiate between synchronous and asynchronous counter?
6. How many no.of flip-flops are required for decade counter?
7. What is meant by excitation table?
8. If the modulus of a counter is 12 how many flip-flops are required?

Experiment -9

MUX- DEMUX APPLICATIONS

Aim:

1. To realize a 4:1 MUX using basic gates.
2. To realize a 1:4 MUX (De MUX) using basic gates.
3. To Realize the given logic expression using 8:1 MUX using IC 74151 $F(A,B,C,D)=\Sigma(2,4,5,7,10,12,14,15)$
4. To realize a Full Adder using 8:1 MUX (IC 74151)
5. To realize a half Subs tractor using 4:1 MUX (IC 74153)

Equipments/ Components Required:-

Name	Specifications/ Range	Quantity
IC	7408	1
	7432	1
	7404	1
	74151	1
	74153	1
Trainer kit	---	1

Theory:-

Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. A simple example of a non electronic circuit of a multiplexer is a single pole multiposition switch. Multiposition switches are widely used in many electronics circuits. However circuits that operate at high speed require the multiplexer to be automatically selected. A mechanical switch cannot perform this task satisfactorily. Therefore, multiplexer used to perform high speed switching are constructed of electronic components. Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates. The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output. Few types of multiplexer are 2-to-1, 4-to-1, 8-to-1, 16-to-1 multiplexer.

Multiplexer are used in various fields where multiple data need to be transmitted using a single line like Communication system, Telephone network, Computer memory and Transmission from the computer system of a satellite. Demultiplexer means one to many. A Demultiplexer is a circuit with one input and many outputs. By applying control signal, we

can steer any input to the output. Few types of Demultiplexer are 1-to 2, 1-to-4, 1-to-8 and 1 to 16 Demultiplexer. The main application area of Demultiplexer is communication system where multiplexer are used. Most of the communication systems are bidirectional i.e. they function in both ways (transmitting and receiving signals). Hence, for most of the applications, the multiplexer and Demultiplexer work in sync. Demultiplexer is also used for reconstruction of parallel data and ALU circuits.

Realization of Multiplexer-

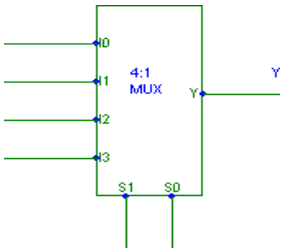


Fig.9.1: 4:1 MUX

Y=S1‟S0‟I0+S1‟S0I1+S1S0‟I2+S1SoI3

TRUTH TABLE

En	**S1S0**	Y
I0	**00**	I0
I1	**01**	I1
I2	**10**	I2
I3	**11**	I3

Circuit Diagram:-

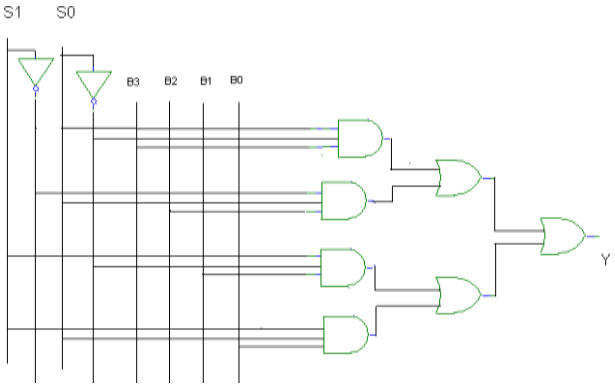


Fig.9.2: 4: 1 Multiplexer

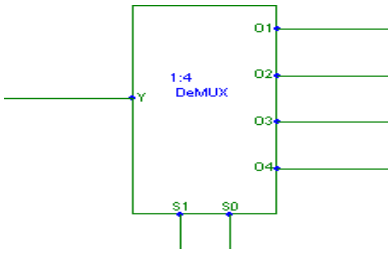


Fig.9.3: 1:4 DEMUX

EQUATIONS

O1=S1‟S0‟D , O2=S1‟S0D , O3=S1S0‟D , O4=S1S0D;

Circuit Diagram:

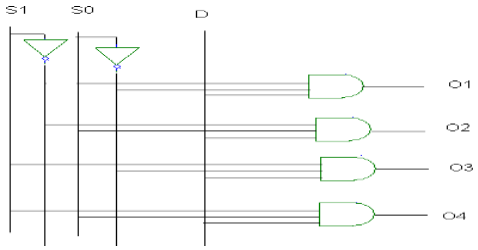


Fig.9.4:1:4 DEMUX

BOOLEAN EXPRESION: f(A,B,C,D)=Σ(2,4,5,7,10,12,14,15)

Truth Table

ABCD	**Y**	**ABC**	**Y**
0000	0	000	0
0001	1		
0010	0	001	D‟
0011	1		
0100	1	010	1
0101	0		
0110	0	011	D
0111	1		
1000	0	100	0
1001	0		
1010	1	101	D‟
1011	0		
1100	1	110	D‟
1101	0		
1110	1	111	1
	1		

Circuit Diagram

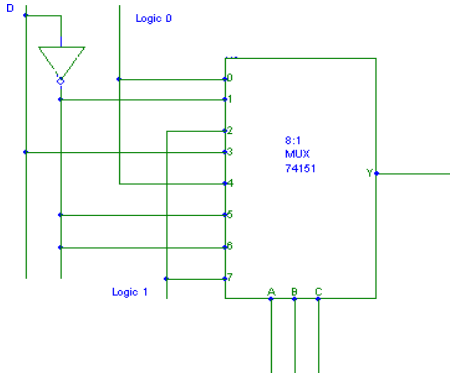


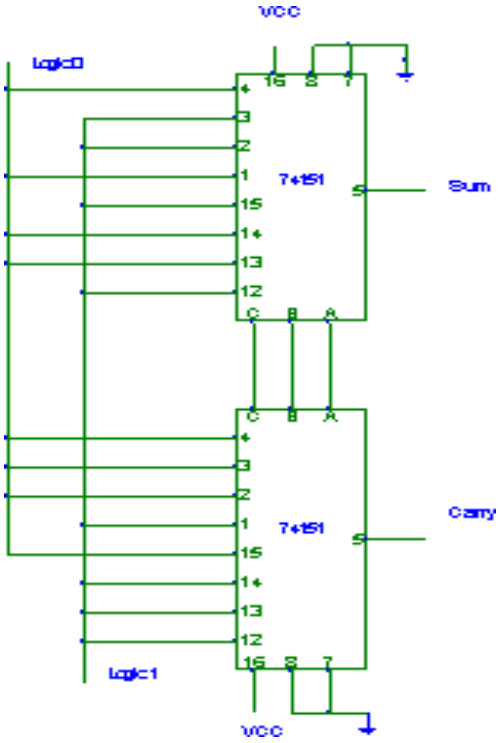
Fig. :

4. Full Adder Using 8:1 Mux (IC 74151):

CBA	S	C
000	0	0
001	1	0
010	1	0
011	0	1
100	1	0
101	0	1
110	0	1
111	1	1

Sum= A‟B‟C+A‟BC‟+AB‟C‟+ABC Carry=A‟BC+AB”C+ABC

Circuit Diagram:

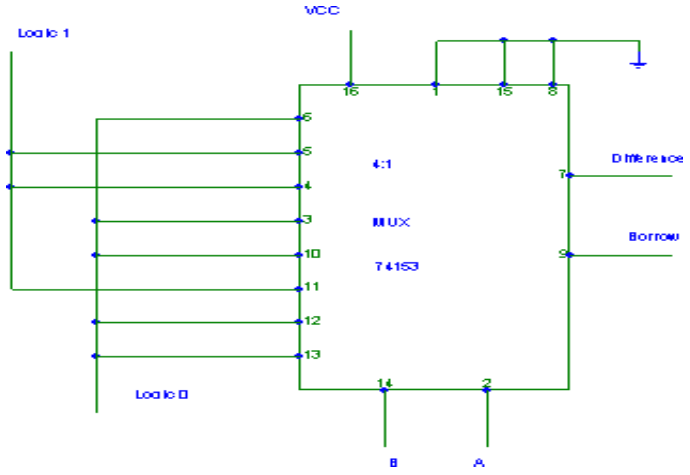


6. Half Subtractor Using IC 74153:

TRUTH TABLE

AB	D	B
00	**0**	**0**
01	**1**	**1**
10	**1**	**0**
11	**0**	**0**

Circuit Diagram



Procedure:-

1. The Connections are made as per the circuit diagram.
2. By giving the different Binary inputs, locate the output such that it matches with the function table of the MUX.
3. Repeat the same procedure for different circuits & take the outputs.

RESULT: - The realization of 4:1 MUX and DeMUX1:4 using basic gates & realization of given function, full adder and half sub tractor is performed and the output is noted and practically verified.

REVIEW QUESTIONS:-

1. What is meant by multiplexer?
2. What are applications of mux?
3. What is demultiplexer?
4. Design 8 input1 output multiplexer?
5. How many 8X1 multiplexers are needed to construct 16X1 multiplexer?
6. Compare decoder with demultiplexer?
7. Design a full adder using 8X1 multiplexer?

Experiment -10

SHIFT REGISTERS AND RING COUNTERS

Aim:- Design of shift registers and ring counters using IC Flip-Flops & Standards IC counters.

Equipments/ Components Required:-

Name	Specifications/ Range	Quantity
IC	7474	1
	7490	1
	74194	1
Trainer Kit		1

Theory:-

Shift registers:

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. All flip-flops are driven by a common clock, and all are set or reset simultaneously**.**

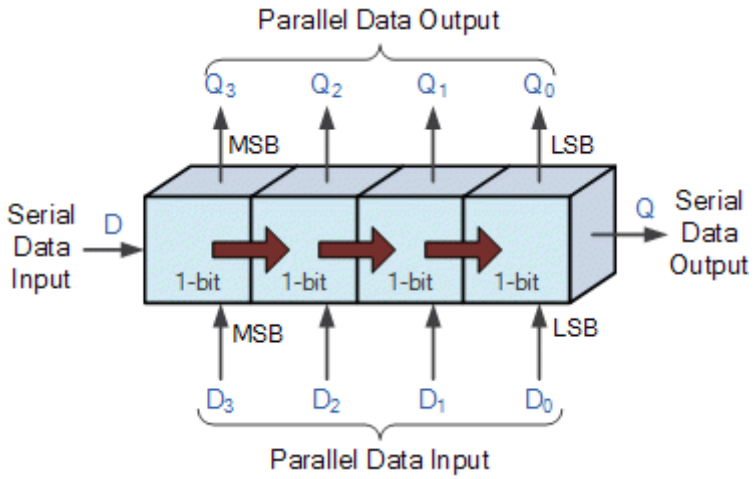


Fig.10.1: Shift Register

1. Serial In - Serial Out Shift Register

The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

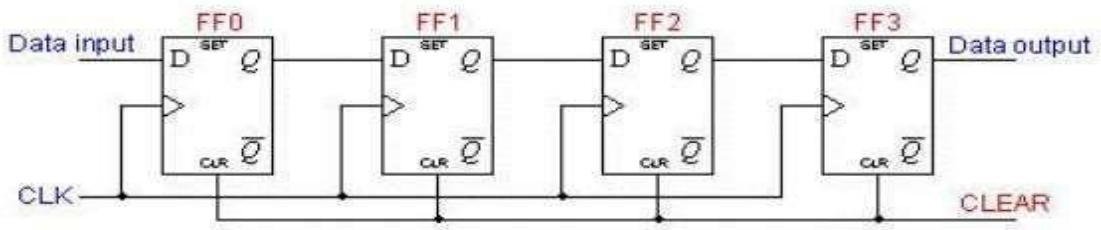


Fig.10.2: Serial In – Serial Out Shift Register

In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. For destructive readout, the original data is lost and at the end of the read cycle, all flip-flops are reset to zero**.**

FF0	FF1	FF2	FF3	
0	0	0	0	1001

The data is loaded to the register when the control line is HIGH (ie WRITE). The data can be shifted out of the register when the control line is LOW (ie READ).

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0

WRITE:

FF0	FF1	FF2	FF3	
1	0	0	1	0000

READ:

FF0	FF1	FF2	FF3	
1	0	0	1	1001

2. Serial In - Parallel Out Shift Register:

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.

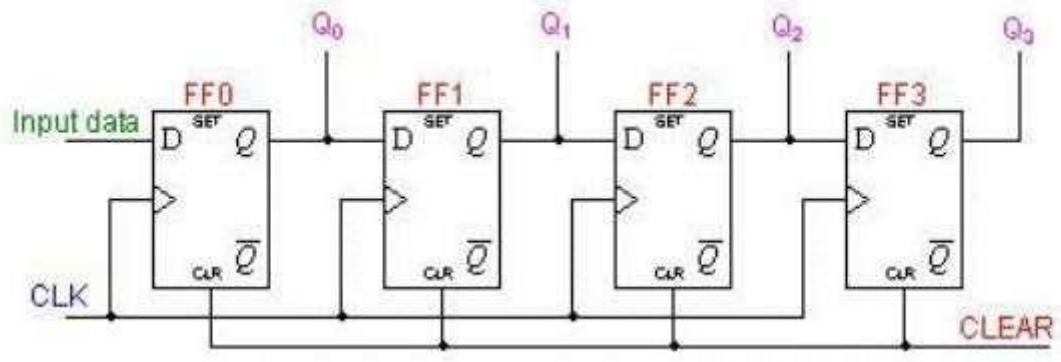


Fig.10.3: Serial In - Parallel Out Shift Register

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

3. Parallel In - Serial Out Shift Register:

A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and NAND gates for entering data (ie writing) to the register. D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse, as shown in the table below.

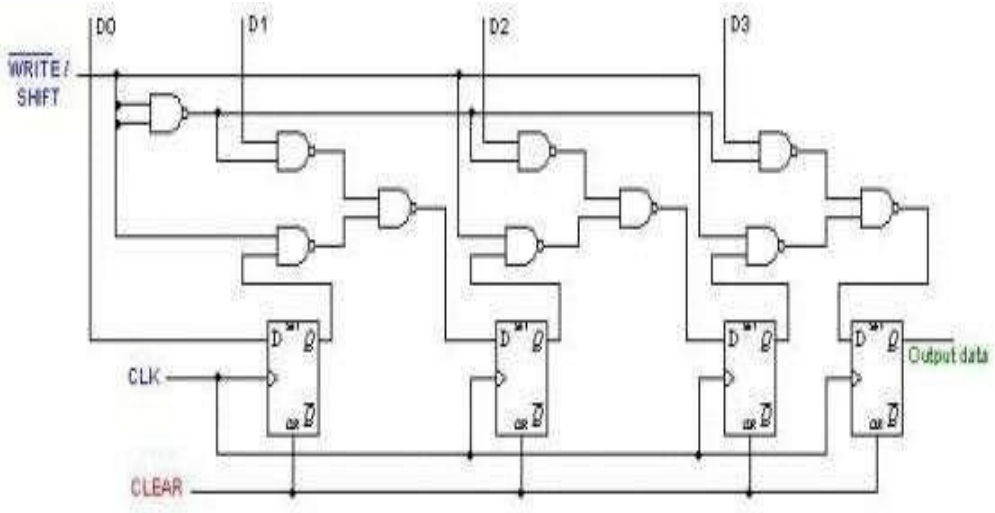


Fig.10.4: Parallel In - Serial Out Shift Registers

	Q_0	Q_1	Q_2	Q_3	
Clear	0	0	0	0	
Write	1	0	0	1	
Shift	1	0	0	1	
	1	1	0	0	1
	1	1	1	0	01
	1	1	1	1	001
	1	1	1	1	1001

4. Parallel In - Parallel Out Shift Register:

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flop. The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

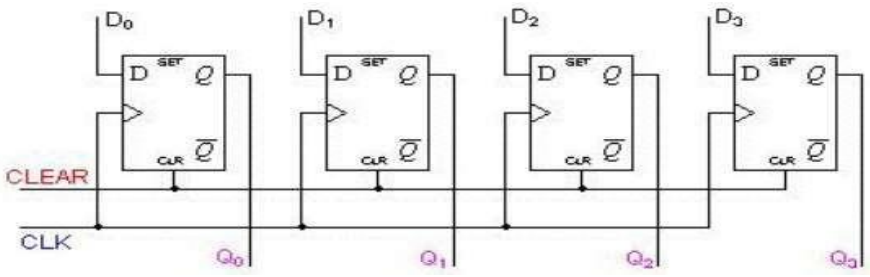


Fig.10.5: Parallel In - Parallel Out Shift Register

5. 4-Bit Bidirectional Universal Shift Registers (74HC194):

The 74HC194 is a universal bi-directional shift register. It has both serial and parallel input and output capability.

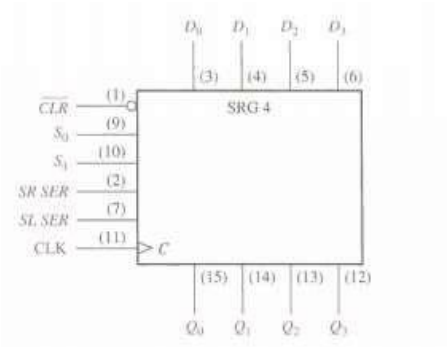


Fig.10.6: 74HC194 4-bit bi-directional universal shift register

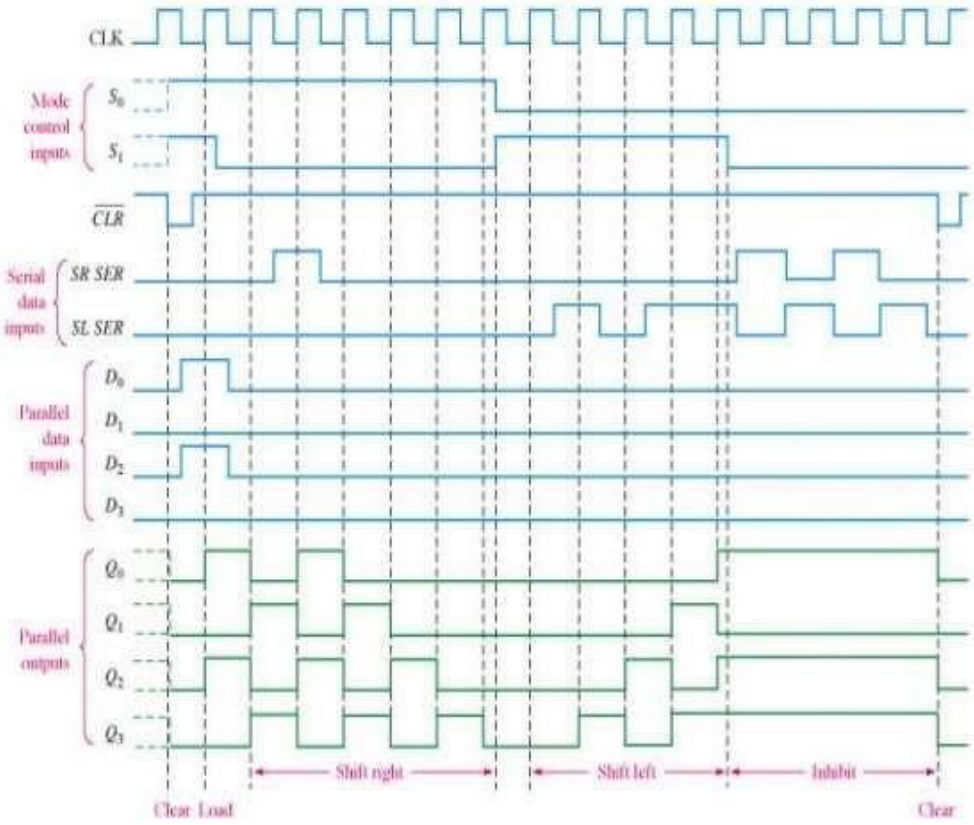


Fig.10.7: The timing diagram of 74HC194

Ring Counters:

A ring counter is basically a circulating shift register in which the output of the most significant stage is fed back to the input of the least significant stage. The following is a 4-bit ring counter constructed from D flip-flops. The output of each stage is shifted into the next stage on the positive edge of a clock pulse. If the CLEAR signal is high, all the flip-flops except the first one FF0 are reset to 0. FF0 is preset to 1 instead.

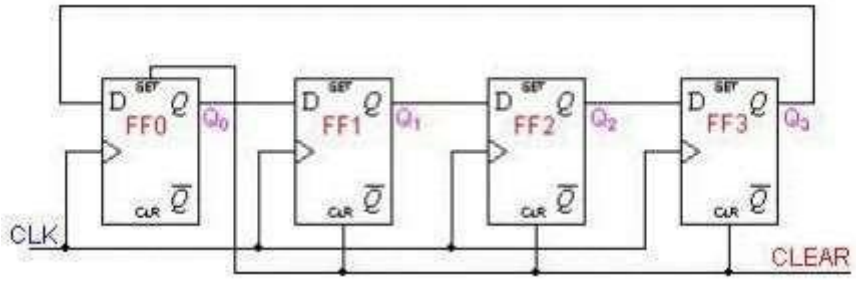


Fig.10.8:Ring Counter

Since the count sequence has 4 distinct states, the counter can be considered as a mod-4 counter. Only 4 of the maximum 16 states are used, making ring counters very inefficient in terms of state usage. But the major advantage of a ring counter over a binary counter is that it is self-decoding. No extra decoding circuit is needed to determine what state the counter is in.

Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0

Johnson Counters

Johnson counters are a variation of standard ring counters, with the inverted output of the last stage fed back to the input of the first stage. They are also known as twisted ring counters. An n- stage Johnson counter yields a count sequence of length 2n, so it may be considered to be a mod- 2n counter. The circuit below shows a 4-bit Johnson counter. The state sequence for the counter is given in the table.

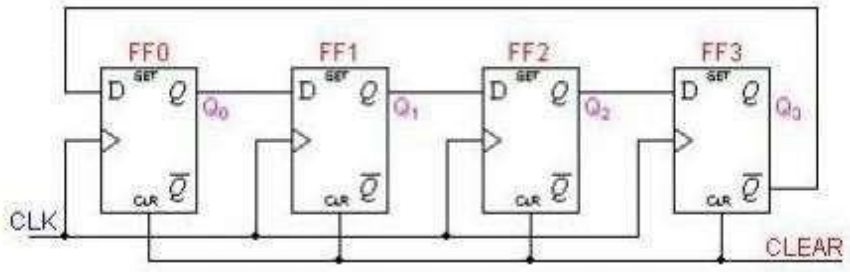
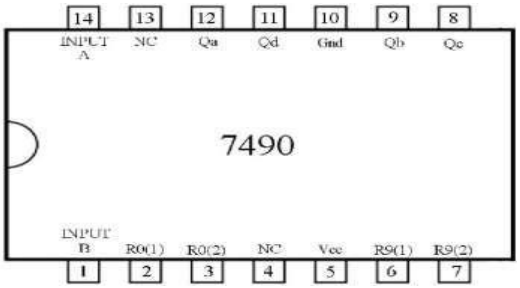


Fig.10.9: Johnson Counter

Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0

Pin Configuration of IC 7490 Decade Counter



Sl. no	Q3	Q2	Q1	Q0
0	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**1**
2	**0**	**0**	**1**	**0**
3	**0**	**0**	**1**	**1**
4	**0**	**1**	**0**	**0**
5	**0**	**1**	**0**	**1**
6	**0**	**1**	**1**	**0**
7	**0**	**1**	**1**	**1**
8	**1**	**0**	**0**	**0**
9	**1**	**0**	**0**	**1**
	0	**0**	**0**	**0**

Procedure:

1. Apply clock to pin 14.
2. Connect either pin 6 or pin 7 to GND
3. Connect either pin 6 or pin 7 to GND
4. Connect pin 12 (Q0) to pin 1 for decade up counter**.**

RESULT:-

REVIEW QUESTIONS:-

1. What is decade counter?
2. How to design modulo-10 counter?
3. What is up-down counter?
4. What is the difference between SISO and SIPO?
5. Draw the timing diagrams for 4 bit input 1010 to SISO

EXPERIMENT 11

CODE CONVERTERS AND PARITY GENERATOR & CHECKER

Aim:- (A) To design and implement a 4-bit Binary to Gray Code converter and Gray to Binary Code converter using logic gates.

(B) To design even and odd parity generator and checker**.**

Equipments/ Components Required:-

1. ICs- 7486.
2. Trainer Kit
3. Connecting wires

Theory:-

(A) Code Converters

Design:-

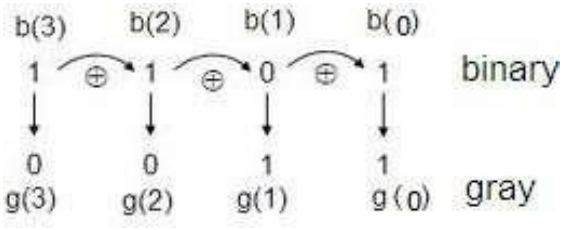
1. Binary to Gray Code converter:

Gray code – also known as **Cyclic Code**, **Reflected Binary Code** (RBC), **Reflected Binary** (RB) or **Grey code** – is defined as an ordering of the binary number system such that each incremental value can only differ by one bit. In gray code, while traversing from one step to another step only one bit in the code group changes. That is to say that two adjacent code numbers differ from each other by only one bit.

Gray code is the most popular of the unit distance codes, but it is not suitable for arithmetic operations. Gray code has some applications in analog to digital converters, as well as being used for error correction in digital communication. Gray code can be difficult to understand initially, but becomes much easier to understand when looking at the gray code tables.

This could have serious consequences for the machine using the information. The Gray code eliminates this problem since only one bit changes its value during any transition between two numbers.

The binary number and the Gray-coded number will have the same number of bits. The conversion process is shown here.



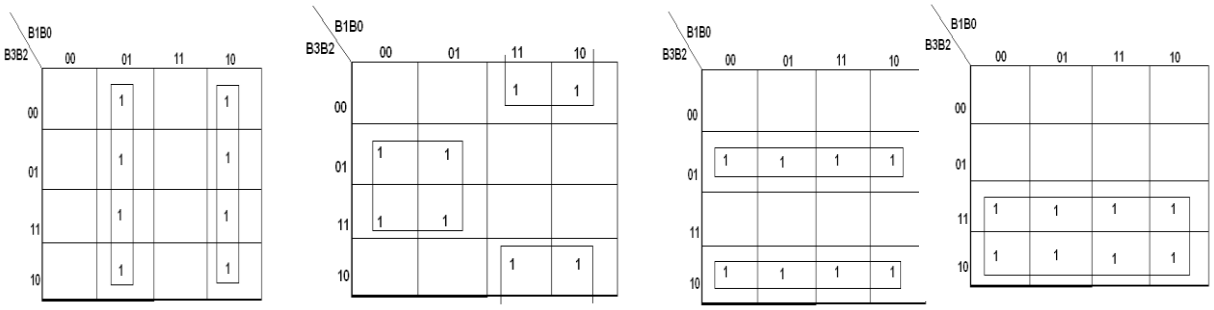
Let B_0, B_1, B_2 and B_3 be the bits representing the binary numbers, where B_0 is the LSB and B_3 is the MSB, and Let G_0, G_1, G_2 and G_3 be the bits representing the gray code of the binary numbers, where G_0 is the LSB and G_3 is the MSB.

The truth table for the conversion is-

Binary Input				**Gray Output**			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**0**	**0**	**0**	**1**	**1**
0	**0**	**1**	**1**	**0**	**0**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**	**1**	**1**	**1**
0	**1**	**1**	**0**	**0**	**1**	**0**	**1**
0	**1**	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**1**	**0**	**0**
1	**0**	**0**	**1**	**1**	**1**	**0**	**1**
1	**0**	**1**	**0**	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**1**	**1**	**0**
1	**1**	**0**	**0**	**1**	**0**	**1**	**0**
1	**1**	**0**	**1**	**1**	**0**	**1**	**1**
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**	**0**	**0**	**0**

To find the corresponding digital circuit, we will use the K-Map technique for each of the gray code bits as output with all of the binary bits as input.

K-map for G_0 **K-map for G_1** **K-map for G_2** **K-map for G_3**



The corresponding minimized boolean expressions for gray code bits –

$G0 = B1 \oplus B0$ $G1 = B1 \oplus B2$ $G2 = B3 \oplus B2$ $G_3 = B_3$

Circuit Diagram:-

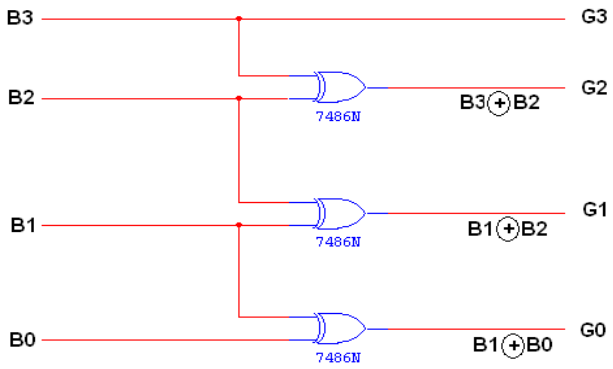
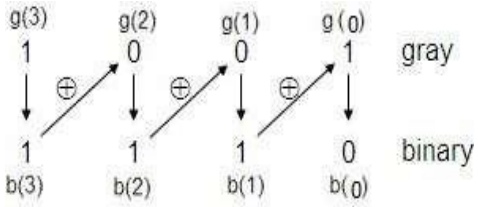


Fig.11.1 : Binary to Gray Code Converter

2. Gray to Binary Code converter:

Converting gray code back to binary can be done in a similar manner. Let B_0, B_1, B_2 and B_3 be the bits representing the binary numbers, where B_0 is the LSB and B_3 is the MSB, and Let G_0, G_1, G_2 and G_3 be the bits representing the gray code of the binary numbers, where G_0 is the LSB and G_3 is the MSB. The binary number and the Gray-coded number will have the same number of bits. The conversion process is shown here.

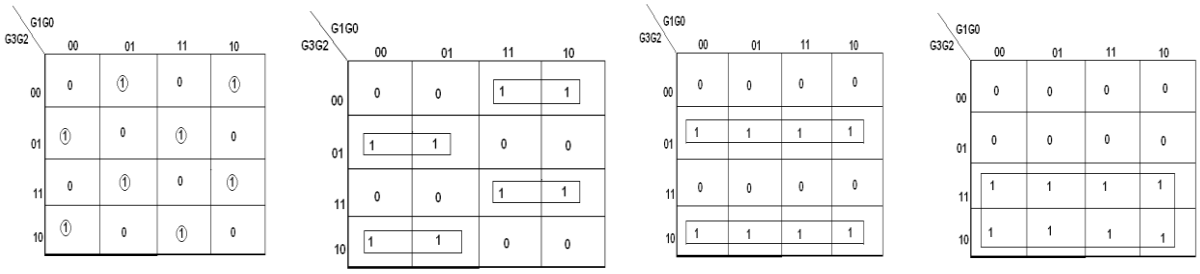


The truth table for the conversion is-

Gray Input				**Binary Output**			
G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**0**	**0**	**0**	**1**	**1**
0	**0**	**1**	**1**	**0**	**0**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**0**	**1**	**1**	**0**
0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
0	**1**	**1**	**1**	**0**	**1**	**0**	**1**
1	**0**	**0**	**0**	**1**	**1**	**1**	**1**
1	**0**	**0**	**1**	**1**	**1**	**1**	**0**
1	**0**	**1**	**0**	**1**	**1**	**0**	**0**
1	**0**	**1**	**1**	**1**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**	**0**	**0**	**0**
1	**1**	**0**	**1**	**1**	**0**	**0**	**1**
1	**1**	**1**	**0**	**1**	**0**	**1**	**1**
1	**1**	**1**	**1**	**1**	**0**	**1**	**0**

To find the corresponding digital circuit, we will use the K-Map technique for each of the gray code bits as output with all of the binary bits as input.

K-map for B_0 **K-map for B_1** **K-map for B_2** **K-map for B_3**



Circuit Diagram:-

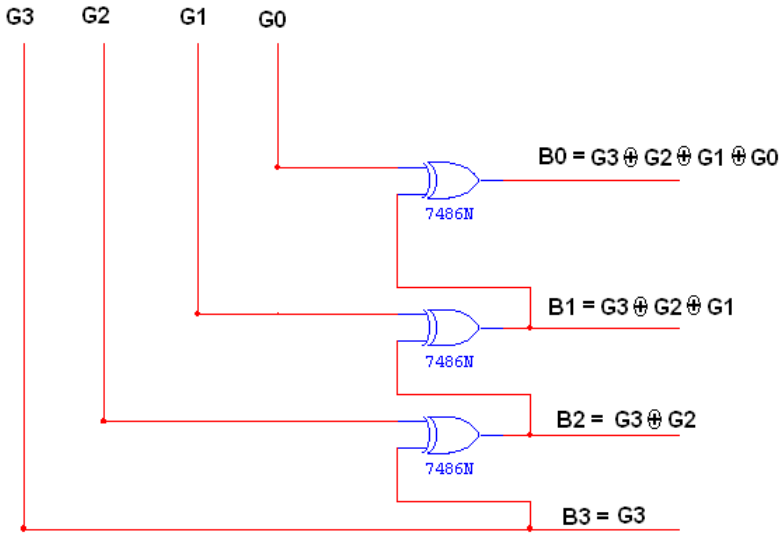


Fig.11.2 : Gray to Binary Code Converter

Parity Generator and Checker

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word. The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even amount whereas in odd parity the added parity bit will make the total number of 1s odd amount.

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

Design of 3 Bit Even Parity Generator:-

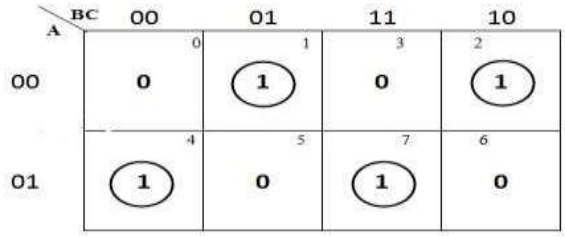
Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuits and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

The figure below shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table of 3 Bit Even Parity Generator

The K-map simplification for 3-bit message even parity generator is,



From the above truth table, the simplified expression of the parity bit can be written as

$$P = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,C$$

$$= \overline{A}\,(\overline{B}\,C + B\,\overline{C}) + A\,(\overline{B}\,\overline{C} + B\,C)$$

$$= \overline{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

Circuit Diagram:

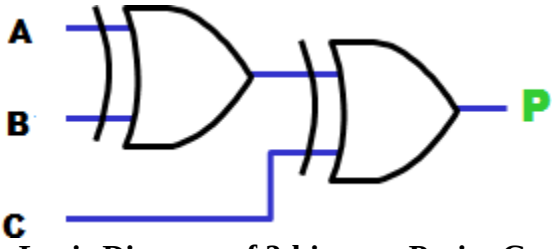


Fig.11.3: Logic Diagram of 3-bit even Parity Generator

3 Bit Odd Parity Generator:-

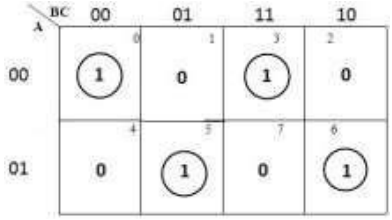
Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table of 3 bit Parity Generator

The truth table of the odd parity generator can be simplified by using K-map as



Circuit Diagram:

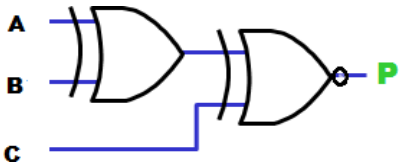


Fig.11.4: Logic Diagram of 3-bit Odd Parity Generator

The output parity bit expression for this generator circuit is obtained as P = A ⊕B Ex-NOR C. The above Boolean expression can be implemented by using one Ex-OR gate and one Ex-NOR gate in order to design a 3-bit odd parity generator.

4 Bit Even Parity Checker:-

Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s. If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

The below table shows the truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-biT message has even number of 1s.

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Truth table of 4-bit even parity Checker

The above truth table can be simplified using K-map. Cp=A⊕B ⊕C ⊕P

The above logic expression for the even parity checker can be implemented by using three Ex- OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.

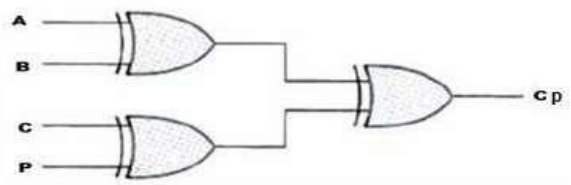


Fig.11.5 : 4-bit Even Parity Checker

4 Bit Odd Parity Checker:-

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4 bits and checks whether any error are present in the data. If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.

The below figure shows the truth table for odd parity generator where Cp =1 if the 4-bit message received consists of even number of 1s (hence the error occurred) and Cp= 0 if the message contains odd number of 1s (that means no error).

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Truth Table Of 4 Bit Odd Parity Checker

The expression for the PEC in the above truth table can be simplified by K-map**.**

Cp = (A Ex-NOR B) Ex-NOR (C Ex-NOR P)

Circuit Diagram:

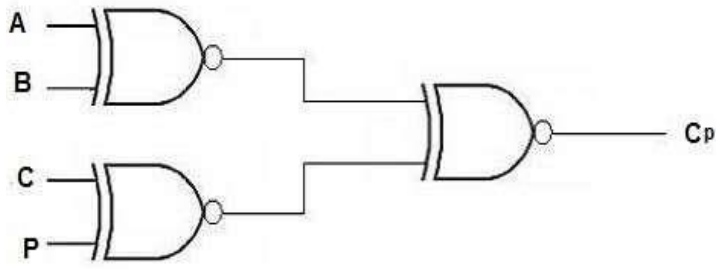


Fig.11.6: 4 Bit Odd Parity Checker

Procedure:-

Code Converters:-

1. The connections are made as per the circuit diagram
2. Give different inputs and observe the outputs.
3. Compare them with truth table. Repeat the same for gray to binary and BCD to Excess-3.

Parity generator and checker:-

1. The connections are made as per the circuit diagram
2. Give different inputs and observe the outputs.
3. Compare them with truth table

Result: -The truth table of logic gates has been verified and the realization of Binary to Gray and Gray to Binary code converter, even and odd parity generator and checker has been done and practically verified.

Review Questions:

1. What are basic gates?
2. What are universal gates?
3. What two logics are considered the most versatile logic gates?
4. Which of the two input logic gate can be used to implement an inverter?
5. What are the applications of code converters and parity checker**?**
6. What is the significance of parity bit?

Experiment 12

Schmitt Trigger Circuits using IC 741 & IC 555

Aim: To design the Schmitt trigger circuit using IC 741 and IC 555

Equipments/ Components required:

Name	Specifications/ Range	Quantity
IC	µA741	1
	555	1
Cathode Ray Oscilloscope		1
DMM		1
Resistor	100 Ω, ¼ W	
	56 KΩ, ¼ W	
Capacitor	0.1 µf, 0.01 µf	

Theory:

Schmitt trigger converts arbitrary wave forms to a square wave or pulse. The circuit is also known as the squaring circuit. The input voltage V_{in} changes the state of the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{ut} and lower threshold voltage V_{lt}. When V_o= - V_{sat}, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}. When V_o=+V_{sat}, the voltage across R_1 is referred to as upper threshold voltage Vut. The comparator with positive feedback is said to exhibit hysteresis, a dead band condition.

Design:

Vutp = [R1/(R1+R2)](+Vsat)

Vltp= [R_1/(R_1+R_2)](-V_{sat})

Vhy= V_{utp} - V_{ltp}

= [R_1/(R_1+R_2)] [+V_{sat} - (-V_{sat})]

Circuit Diagram of Schmitt trigger circuit using IC 741:

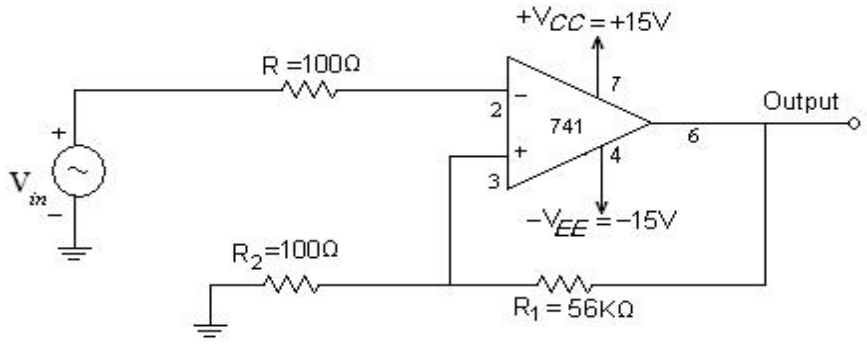


Fig.12.1 :Schmitt trigger circuit using IC 741

Procedure:

1. Connect the circuit as shown in Fig 12.1.

2. Apply an arbitrary waveform (sine / triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.

3. Observe the output at pin6 of the IC 741 and by varying the input and note down the readings as shown in Table 1 and Table 2.

4. Find the upper and lower threshold voltages (V_{utp}, V_{Ltp}) from the output wave form.

Circuit Diagram of Schmitt trigger circuit using IC 555:

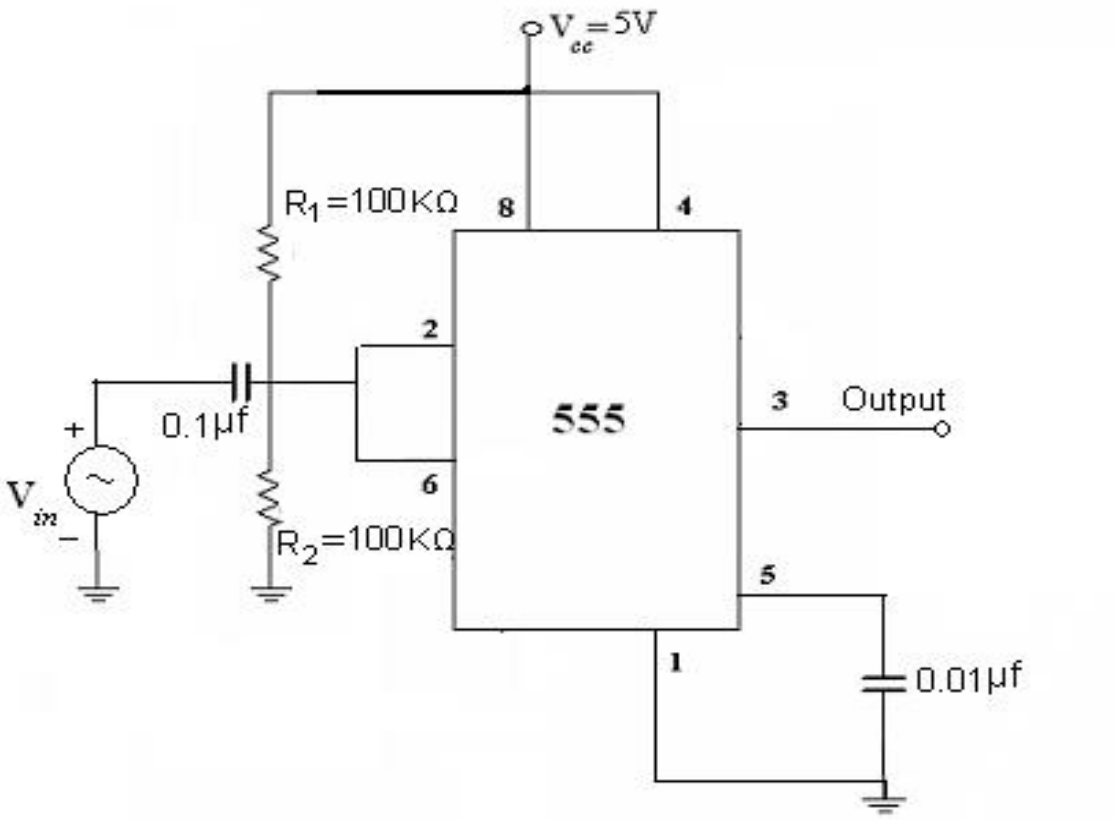


Fig.12.2 :Schmitt trigger circuit using IC 555

Procedure:

1. Connect the circuit as shown in Fig 12.2.

2. Apply an arbitrary waveform (sine / triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.

3. Observe the output at pin 3 of the IC 555 and by varying the input and note down the readings.

4. Find the upper and lower threshold voltages (V_{utp}, V_{Ltp}) from the output wave form.

Expected Wave forms:

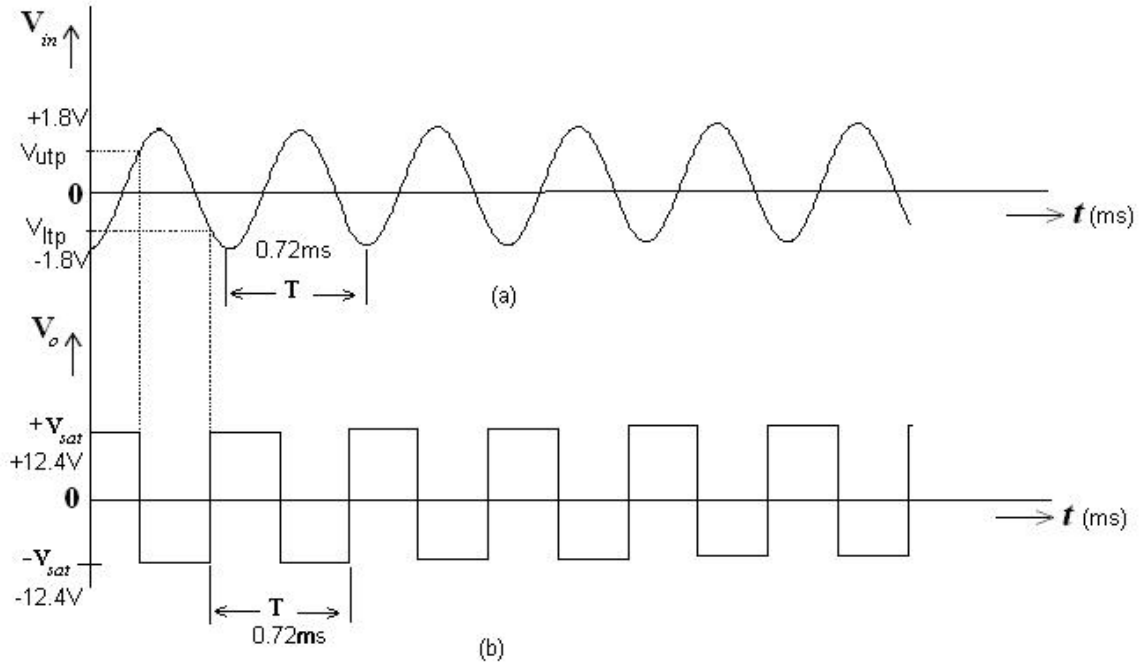


Fig.12.3 : Input and Output Waveforms of Schmitt trigger

Observations & Calculations:-

Parameter	**Input**		**Output**	
	741	555	741	555
Voltage(V_{p-p})				
Time period(ms)				
Parameter	IC 741		IC555	
V_{utp}				
V_{ltp}				

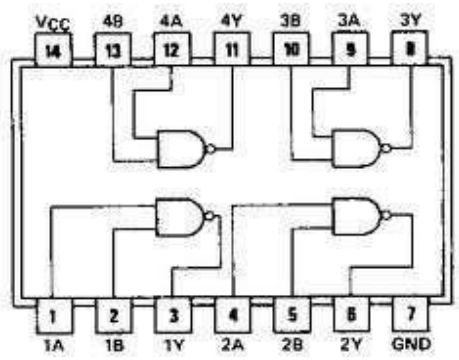
Results:

UTP and LTP of the Schmitt trigger are obtained by using IC 741 and IC 555.

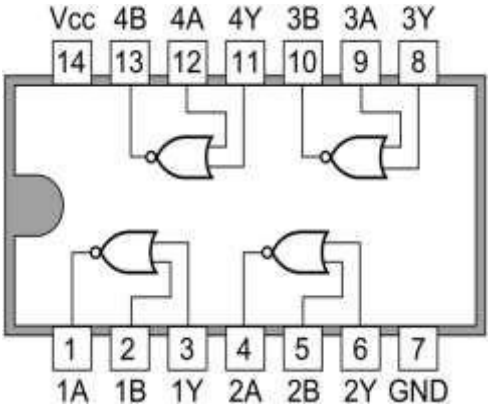
Inference: Schmitt trigger produces square waveform from a given signal.

PIN CONFIGURATIONS

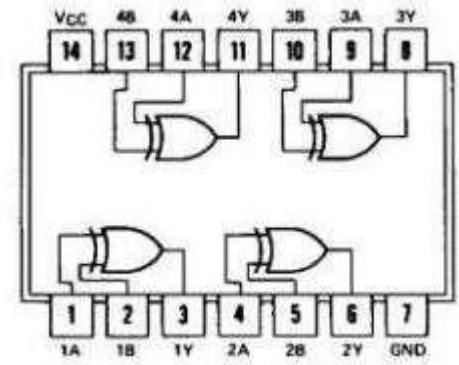
IC 7400-2 INPUT NAND GATE



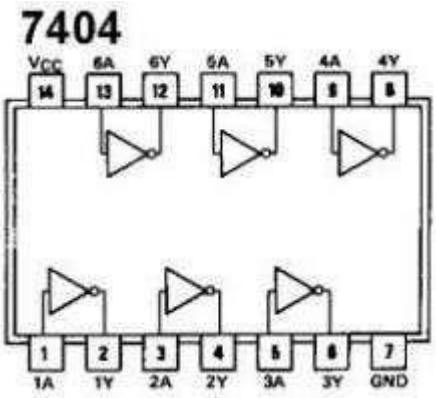
IC 7402-2 INPUT NOR GATE



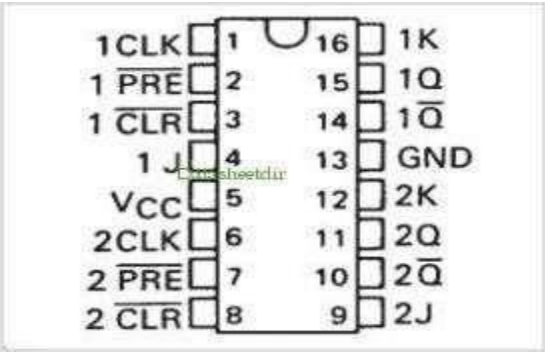
IC 7486-2 INPUT EX-OR GATE



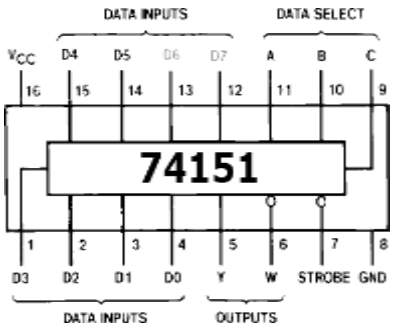
IC 7404-NOT GATE



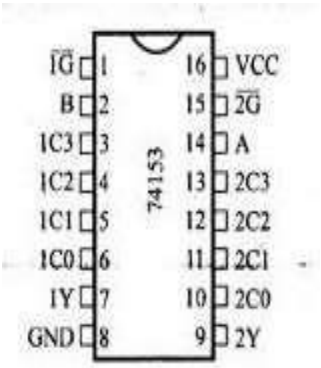
IC 7476 JK FLIPFLOP



IC 74151



IC 74153


1G 1
B 2
1C3 3
1C2 4
1C1 5
1C0 6
1Y 7
GND 8
74153
16 VCC
15 2G
14 A
13 2C3
12 2C2
11 2C1
10 2C0
9 2Y